ModEasy Kick Off meeting

10 February 2005

Welcome in Lille

30 seconds to present yourself!!

iemn Recherche C.N.R.S.

KENT
UNIVERSITY OF KENT

INRIA FUTURS

Agenda

10h30 Introduction – presentation - JLD

10h45 Inria :

- Profile and metamodel: Arnaud
- Model Driven Architecure :Lossan
- Power consumption: Smail

11h30 Kent

12h45 Lunch

15h00 IEMN

15h30 Scientific collaborations

16h00 Administrative aspects

16h30 The End

ModEasy

MOdel Driven dEsign for Automotive Safety embedded sYstem

- « Modélisation, vérification de systèmes de sécurité pour des systèmes embarqués dans l'automobile »
- Tools and techniques to aid in the development of reliable embedded systems
  - general-purpose development and verification systems.

Ideas

The design process of embedded systems moves

- from abstract high level descriptions (models) such as block diagrams,
- to low level specific implementations details (microchip circuit diagram).

To create a bridge between the high level abstract description (specification co-design systems) and the low level implementation details (synthesis co-design) on various hardware platforms.

To do…

To survey typical requirements for embedded systems development in industry.

To propose formalised models *(metamodels*) for the structure and the behaviour of the high level descriptive models.

To define metamodels for lower level implementation details (on platforms such as SystemC, RTL and VHDL in MOF)

To define the transformation rules

To design for each of these models a corresponding software tool allowing a rapid and accurate performance evaluation.

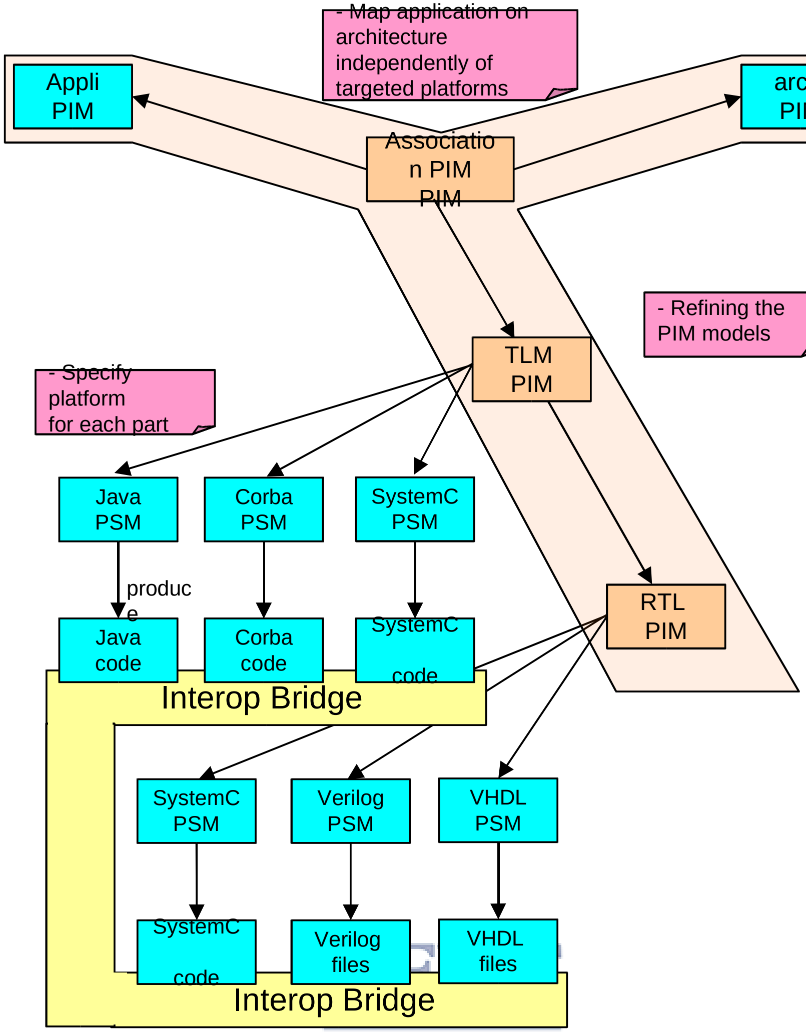
The design and construction of a verification tool (based on formal mathematical logic) for the transformations from high level UML to the specific platform, e.g. SystemC or VHDL.

Investigating the implementation of the models in reprogrammable microchips (i.e. Field Programmable Gate Arrays - FPGAs).

To evaluate the system for pre-commercial industrial applications.

To implement the prototype systems on FPGAs, and examine the feasibility of implementing it as not reprogrammable chip

GasPard Platform



Cruise control with GPS

Modelling a cruise control connected to the satellite positioning system, GPS: The speed limit will be automatically obtained from the position of the car and the data base use for itinerary processing. It will no longer be possible to select a cruise speed higher than the speed limit. This limit information can be updated with the RDS/TMC option via the incar enterntainment system (i.e. radio).

Modelling and verifying the specification of the system from a UML specification and using classical verification and model checking techniques to assure the correct behaviour of the system. Using model transformation allows the guarantee of these verifications at the lower levels like SystemC/VHDL.

Radar anti-collision

The collision avoidance radar has been built in the 10 GHz band and then in the 60 GHz one (reserved for vehicles safety applications).

Range of 150 m has been measured using 200 mW of emitted power for radars embedded on test vehicles on highways.

The receiver uses digital correlators which have been implemented via DSP microprocessors.

The codes are generated using FPGA devices.

seeking to design the major parts as embedded systems based on FPGA and SoC devices.

- easier expansion of the system by adding new advanced algorithms,.
- improve and facilitate the design of such complex system.
- new algorithms or new FPGA's can rapidly be integrated in the system by the re-use of existing functional blocks.

Action list today

- Scientific committee
  - Industrials
  - Academics
  - Schedule
- Web site
  - Inria Webmaster Philippe

Action list today

- Mailing list
  - modeasy@kent.ac.uk
- Scientific meeting schedule
  - Different topics
    - MDA : INria /Kent : Luc Charrest + Arnaud Cuccuru
    - Application : Iemn + Inria + Kent : Attika Rivencq
    - Verification : Inria / kent : Gareth + Eric Rutten
    - Simualtion : Inria + Kent : Smail Niar
    - Synthesis : Kent + Inria Klaus McDonald- Maier
  - Schedunling
    - 4 a year
    - Call on mailing list
    - Minutes on the web site
  - Plenary meeting every year in june

Action list today

- Student exchange
  - 2 weeks trip
- Researcher exchange
  - Invited Professor???? Lille and valenciennes (1 to 6 months) Industrial?????
  - England funding?????
- Communication / Logo / Slides

Workpackage 1: Investigation of the Problem (T+0 to T+8, Leader: INRIA)

Study of the existing UML Profile for Real-time and Embedded systems (INRIA)

Evaluation of the MDA tools (INRIA)

Study of the new features of UML2.0 to express data flow and control flow (INRIA)

Verification techniques and Activity/sequence diagram in UML2.0 (INRIA / Kent)

Synchronous techniques in UML2.0 (INRIA)

Observation of IP Interface standard development (Spirit project) (INRIA / Kent)

Cruise control specifications (INRIA / Kent)

GPS navigator characteristics (IEMN / INRIA / Kent)

Anti-collision radar specifications (IEMN)

Investigation into SystemC to VHDL transformation tools (Kent)

Survey of SystemC and VHDL design flow for embedded system development with FPGAs (Kent)

Survey of related formal verification approaches (Kent)

Deliverables:

Reports covering the above points, i.e. **(June 05)**

- Model, transformation and verification
- Application domain characteristics and requirements
- SystemC, VHDL and FPGA synthesis

Workpackage 2: Model Driven Engeneering (T+3 to T+24, Leader: INRIA)

Application metamodel for data flow and control flow and UML Profile

Hardware metatmodel and UML profile

Verification of the behaviour

IP integration

Mapping metamodel and UML profile

Debugging in a multimodel system

Standardisation effort to OMG

Transformation techniques (INRIA)

Model based verification guarantee during transformations (INRIA / Kent)

Deliverables:

UML profile integrated in UML tool (T+18)

Eclipse environment for model transformation (T+24)

Workpackage 3: VHDL/SystemC Models and Verification Tools (T+3 to T+36, Leader: Kent)

SystemC, RTL metamodel and tranformation rules (INRIA / Kent)
VHDL metamodel (INRIA / Kent)
FPGA generation from models (Kent)
Design of formal models for design metamodels (Kent)
Investigation of formal methods of modelling SystemC and VHDL (Kent)
Generation of tools for SystemC and VHDL formal verification (Kent)

Deliverables:

Prototype verification tool for SystemC (T+18)
Refined verification tool for SystemC (T+36)
Prototype verification tool for VHDL (T+36)
Prototype tool for SystemC generation from UML (T+24)
Full integration in Eclipse environment (T+36)

Workpackage 4: Evaluation using Specific Practical Applications (T+8 to T+36, Leader: IEMN,)

Cruise Control and GPS

To model the application of the Hardware of the SoC and its mapping. (INRIA / Kent)

To apply the transformation rules (INRIA / Kent)

To generate the RTL (Kent)

To realise an embedded systems implementation with FPGAs (Kent)

To integrate the system in a GPS environment (INRIA / Kent)

Anti-collision radar

To model the application of the Hardware of the SoC and its mapping. (INRIA / IEMN) with digital (multibit) correlator, one bit correlator and higher order estimators

To apply the transformation rules (INRIA / IEMN)

To generate the RTL (IEMN/Kent)

To realise an embedded systems implementation with FPGAs (IEMN/Kent)

To evaluate the system in a test road vehicle (IEMN

Deliverables:

Application model and definition specification (T+18)

Two FPGA prototype implementations (T+24)

Two refined FPGA implementations (T+36)

Report on the evaluation of prototype and refined systems (T+36)

Workpackage 5: System-on-a-Chip Co-model Investigation (T+24 to T+36, Leader: Kent)

A study will be carried out into the feasibility of a complete single chip system using leading-edge SoC technology. (INRIA / Kent).

Deliverables:

Report detailing the results (T+36)

Dissemination (T+6 to T+36)

Courses at University of Lille

Publications

Seminars and workshops

Calendar

Mid-April in Valenciennes

Mid-June + plenary in Canterbury

Workshop in June 2006????

To do

Action	Date	Who?
Slide on the Web	28/02	All speakers->webmaster??
Papers sharing	Anytime	All
Record on topic groups	28/2	all
Logo	Tomorrow	Luc
List of email dha@kent.ac.uk	Next week	Atika and JLD
Official logo etc	End february	Atika
Workshop (organisation + funding) FDL'06	June	atika
Brime tech	march	Smail
Inria automotive		Eric / JL
STmicro	March	Eric
England partners???		Gareth
Inrets	march	Atika Yassin
Delphi	March	Klaus