ModEASY

Kent Team
+ Background
+ Plans

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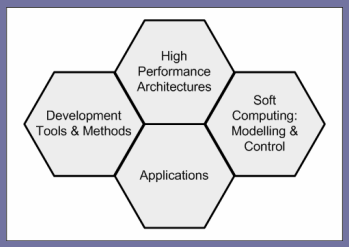
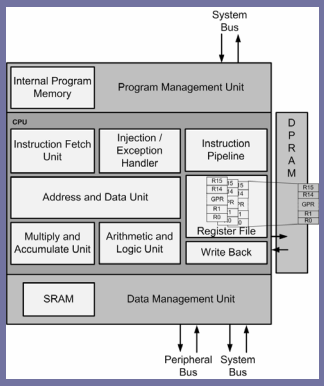
Overview



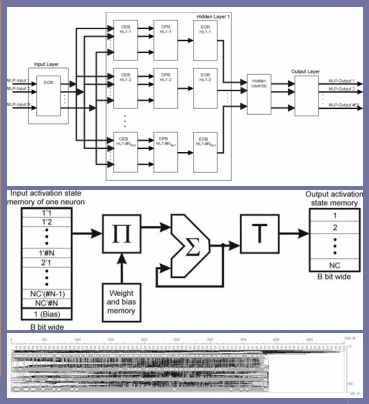
- Extracting Parallelism from Language and Problem domains
- Neural and Embedded Systems Hardware Architectures
- Robot Movement Control
- Neural Networks
- Image Processing and Pattern Recognition
- Multimedia Document Design and Analysis
- Biometric based security

High Performance Architectures: SoCs



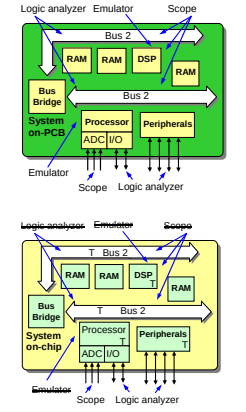
- C166S Vx & Tricore 2
  - MCU & DSP
  - Reusable Cores + System IP
  - Performance lead
  - Real-time embedded SoCs, e.g.:
    - Mobile and fixed comms.
    - Automotive control
    - Consumer
- Current focus
  - SoCs for distributed sensor networks / image processing
    - High performance
      - Parallel execution
      - Neural Networks
    - Low power / power awareness
    - Reconfigurability
      - Processor node
      - Network topology

High Performance Architectures: Optoelectronic Processing



- Electronic processing
  - High precision
  - Low interference
- Optical communications
  - Flip-chip bonded VCSEL / SEED senders and receivers
  - optical interconnect
- Benefits:
  - High fan outs possible (80+)
  - Fast, precise & high bandwidth
- Performance
  - increase up to factor **100** shown for NN and transform processors!
- Current focus:
  - SoC external communication interface
  - on-chip and chip-to-chip based Network-on-Chip architectures

Debug Support: The Embedded SoC Challenge

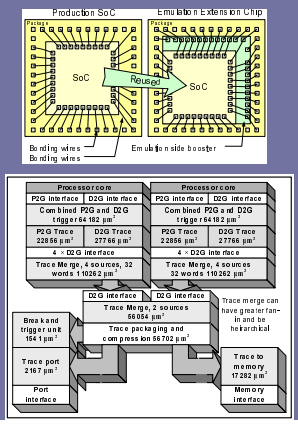


The Challenge:
- End user wants a bug free product
- Electronic systems are getting ever more complex
  - 10 million transistors per chip
  - 10 million lines of code SW
  - 100 microcontrollers per car
  - Mixed technologies and signals
  - Harsh and difficult to model environments

Bug Fixing:
- 1. Observe, 2. Analyze, 3. Fix

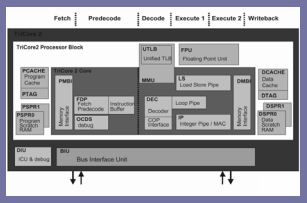
Approaches:
- Run time control
  - Classical breakpoint debugging for software
  - Snapshot of system states
- Modeling / FPGA Emulation
  - very useful in the early system development phase for debugging
- *Run time control and tracing in the target system*
  - Overcomes all limitations of run time control only
  - Allows to observe and analyze all system states in parallel on a time scale
  - However cost of trace pins, memory and equipment imposes restrictions on the visibility of system states

SoC Development Methodology



- Novel debug methodology and infrastructures:
  - Very low hardware overheads
    - SoC external interface
    - On chip size
    - Two chip solutions
    - Debug support IP
  - Improved compression
  - Multiple core solution:
    - compatible with most SoC architectures
    - supports emerging Network-on-Chip architectures

Determinism and Processors with Cache



- Problem:
  - Modern processors use Performance Boosters:
    - Cache
    - (Pipeling)

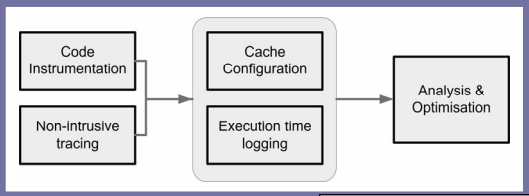
  => Variance in execution time

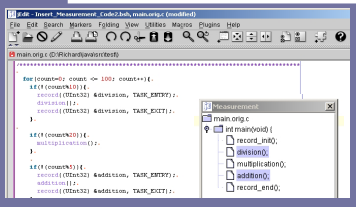
  => Reduced level of Determinism

  => Critical for hard real-time systems!
- Current solution:
  - Cache => switched off
  - (Pipeling => handled by compiler)

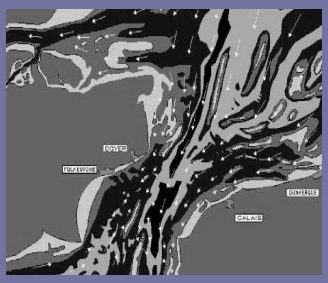
'buy a sports car and drive it in first gear'

Performance Measurement and Analysis



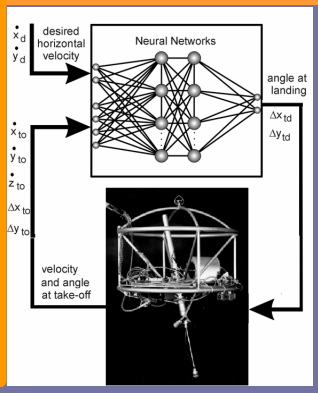


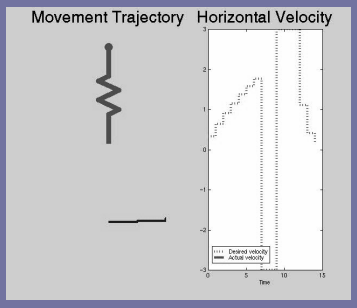
ACOS - Automated Control and Guidance System



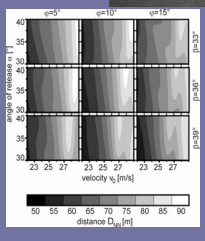
- with ISEN Lille, SIMRAD, RDDS

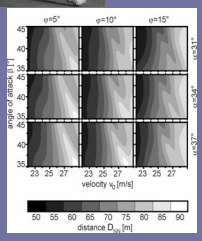
Neural Networks for Robot Movement Control





Neural Modelling and Applications





- Computational modelling of mechanisms in the mammalian visual cortex
  - with Univ. Newcastle, ClearSpeed
- IRIS : Image retrieval for industrial and medical systems
  - with CREA Amiens, K&C, ...
- Computational modeling of mechanisms in human physiology
  - with Univ. Essex
- ITSS - An intelligent toolset for sports science analysis using pattern analysis
  - with Univ. Essex

Parallel Processing

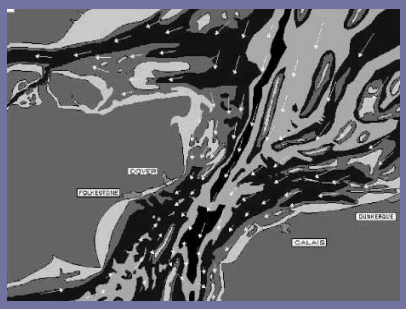
- Experience of extracting parallelism from Declarative languages
- Video Processing architectures
- Interested in extracting parallelism from problem domains for use on custom hardware

Logic Based Networks

- Conventional Computer Programs will repeat a mistake if presented with the same data
- Artificial Neural Networks seek to learn and generalise from their data to avoid the above
- Conventional neural networks are however:-
  - Slow at learning
  - Computationally intensive to implement
- Work at Kent seeks to:-
  - Generalise the traditional structure of networks
  - Include formal logic concepts to allow greater analysis

Example Problem Domain

- Dover Harbour Model
- Real World Problem
- Large Quantities of Data
- Multi-dimensional Nature of problem



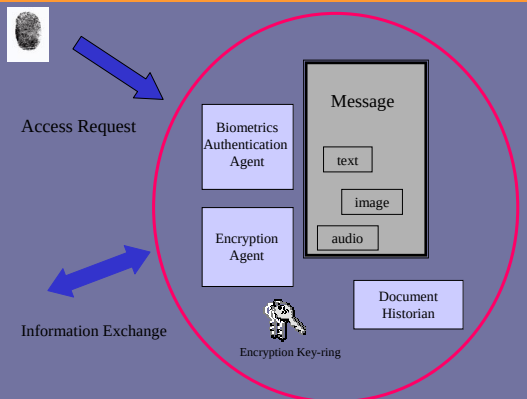
RAM –based Networks

- Number of Architectures designed at Kent
  - BCN, GCN, PCN
- Using such neurons allows
  - one shot learning (no need to perform thousands of learning iterations)
  - arbitrary input to output mappings (XOR poses no special problems)
  - easier direct hardware implementations (no floating point operations)

Fuzzy Networks

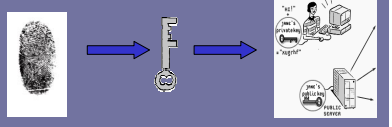
- Fuzzy ARTMAP: a ART-Based neural networks with two ART modules and supervised learning
- RePART: a variation of Fuzzy ARTMAP with a reward/punishment process
- RePART has already been investigated with other ARTMAP-based models
- A comparative analysis of RePART performance with Fuzzy Multi-layer Perceptron and RAM Radial

Documents as Autonomous Objects

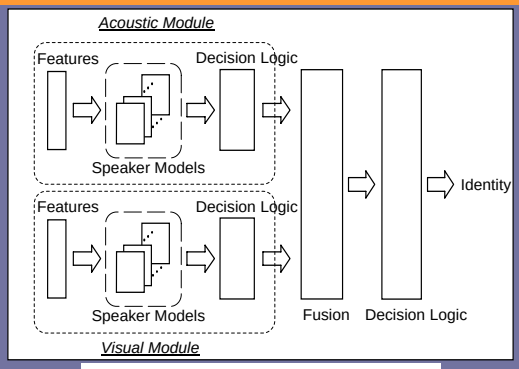


Bio-Encryption

- Convenience
  - Readily available
  - Not possible to misplace
- Uniqueness
- Security
  - Difficult to Steal / Forge
- Biometric Integration
  - encryption keys are released through biometrics
  - live biometric traces may be embedded within documents for authenticity and non-repudiation



Multi-Expert Systems



Post-categorical Integration

Medical Applications

- Non-Invasive Medical Instrumentation
  - Dysgraphia
  - Mammography
  - Visio-Spatial Neglect