



High Level Power Consumption Co-estimation in the MODEASY Project

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Power Consumption in SOC design

- Power consumption considerations will dominate all parts in high end and embedded system designs
- Low power will be the dominant design criteria for SoC – not speed or area.

What is high level co-estimation ?

- High level : To give to the user, at early phases in the design flow, indications concerning the architecture/application performance (power consumption).
- Co-estimation : Hardware and software parts of the design
 - Hardware estimation tool : Compromise between abstraction level (system level) / accuracy (RTL/architectural level)
 - Software estimation tool : application are in High Level Programming OO lang, SystemC, ARRAY_OL,

Power Consumption.....

- What to estimate ? Power consumption;
But Power and performance (time) go hand by hand.
- A fast but accurate power estimator/evaluator
- Dedicated to Intensive signal processing applications : FFT, GSM, MPEG,

Why Early Power Consumption Co-Estimation?

- Decisions made during first stages of conceptions have a big influence on final design performances.
- These estimations/indications permit to explore a large space of solutions
 - to find the best architecture/algorithm respecting constraints.
- Reducing the time to market: reduces the number of loops in the design flow.

Two approaches in power aware design

1. Power Estimation
2. Power reduction techniques

Power Estimation

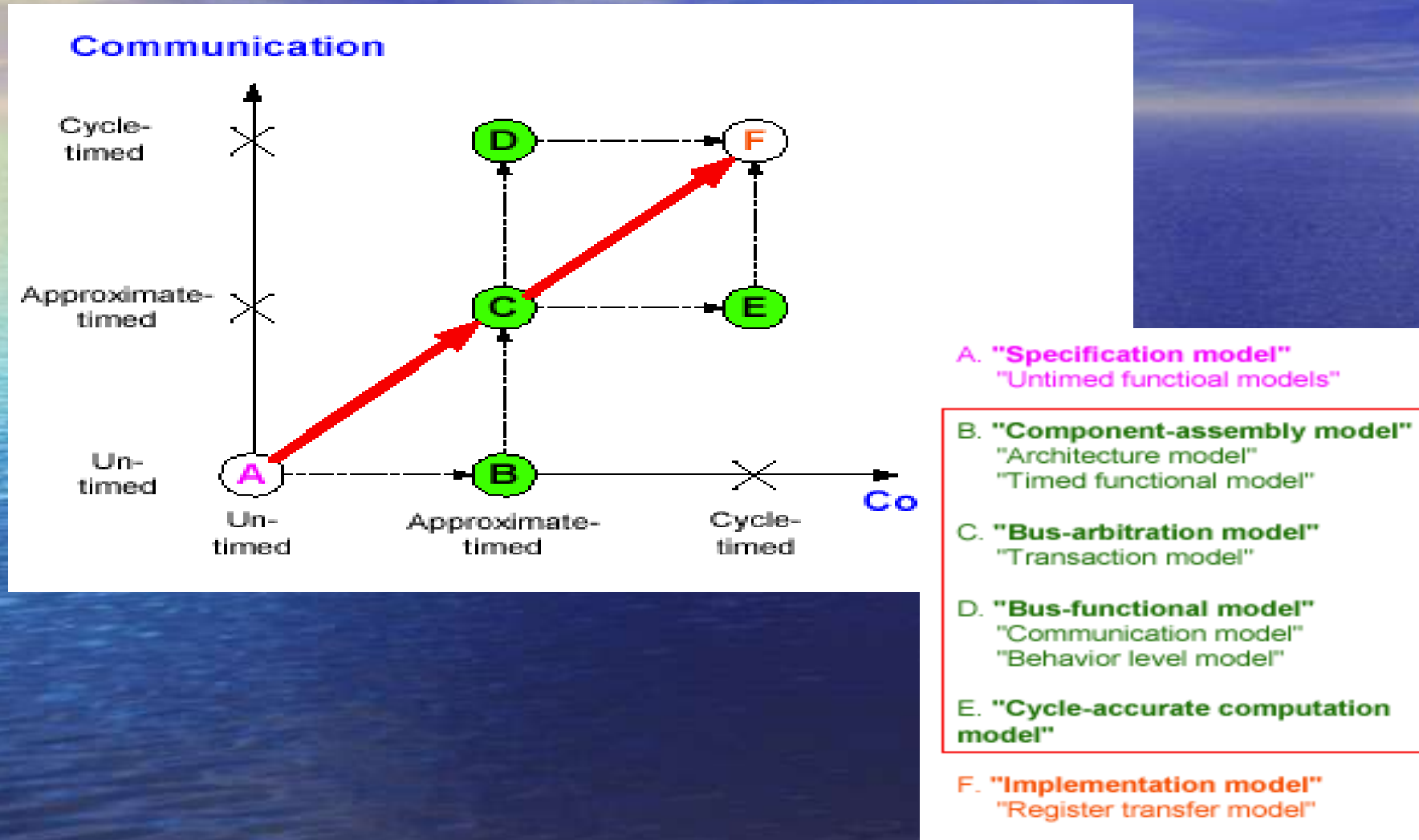
- Design a tool that can estimate the power consumption.
- Requirements of power estimation
 - Fast— to explore a large design space in early stages
 - Retargetable – to evaluate architecture/code alternatives
 - Estimation should have high fidelity

Power reduction techniques

Power = Fct (activity, voltage,
freq)

- **Clock (voltage) reduction**
- **Activity reduction**
- **Static power consumption reduction**

Transaction Level Model TLM



Power Consumption can be Evaluated at different phases using the TLM design approach

Abstraction Level in Power Consumption Evaluation

Functional Level

Processor+Memory+Intercon

TLM Level

Approximate

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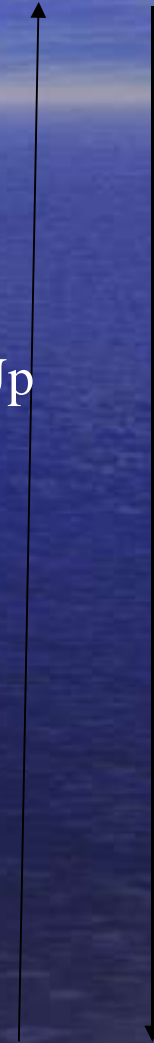
Cycle Accurate Bit Accurate

RTL Level

Transistor

Speed Up

Accuracy



Power Consumption Co-estimation in GASPARD?

