

Application modeling draft

Sébastien LE BEUX
PhD student
lebeux@lifl.fr

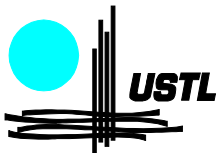
Overview

- Previous meeting
 - 2 meetings on application
 - 1.5 meeting on FPGA
 - 1 meeting on transformation
- Conclusion
 - Application modeling in UML

Summary



- Application part
 - Correlator algorithm
 - HOS 3 algorithm
 - Characterisation
- Architecture part
 - FPGA characterisation



- Application part

Correlator : algorithm side

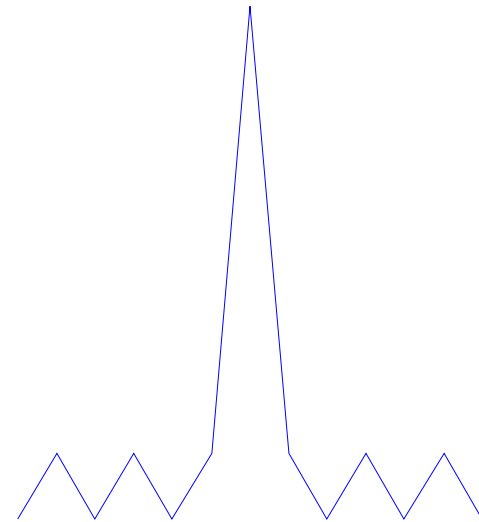
- Objective
 - Compare radar signal with reference signal
 - Detect distance
- Formula

$$S(k) = \sum_{n=0}^{\infty} C^*(n) \cdot D(n+k)$$

S : Distance detection compute

C: Reference signal

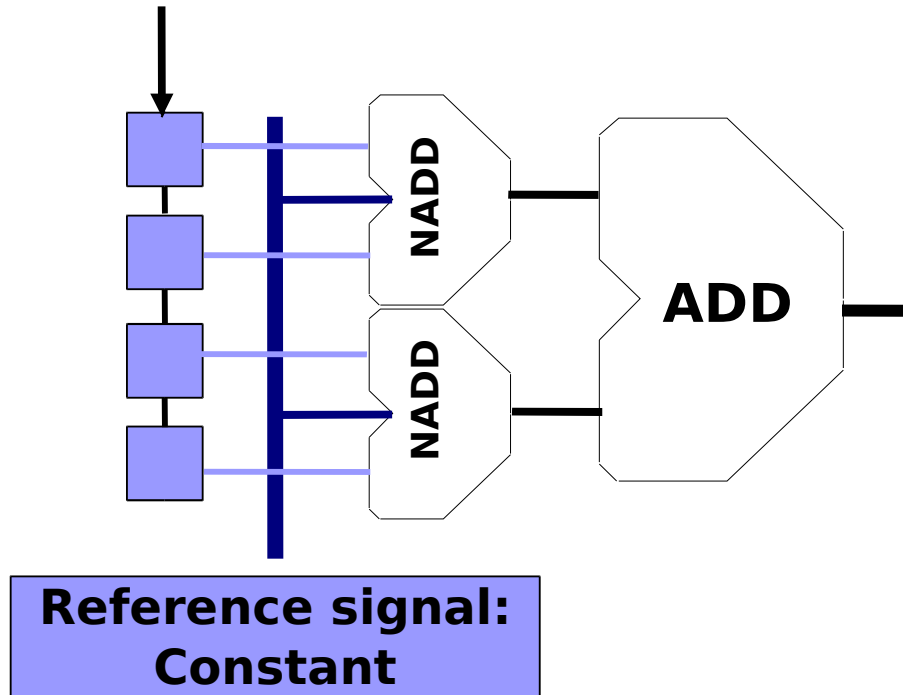
D: Radar signal



Correlator: hardware side

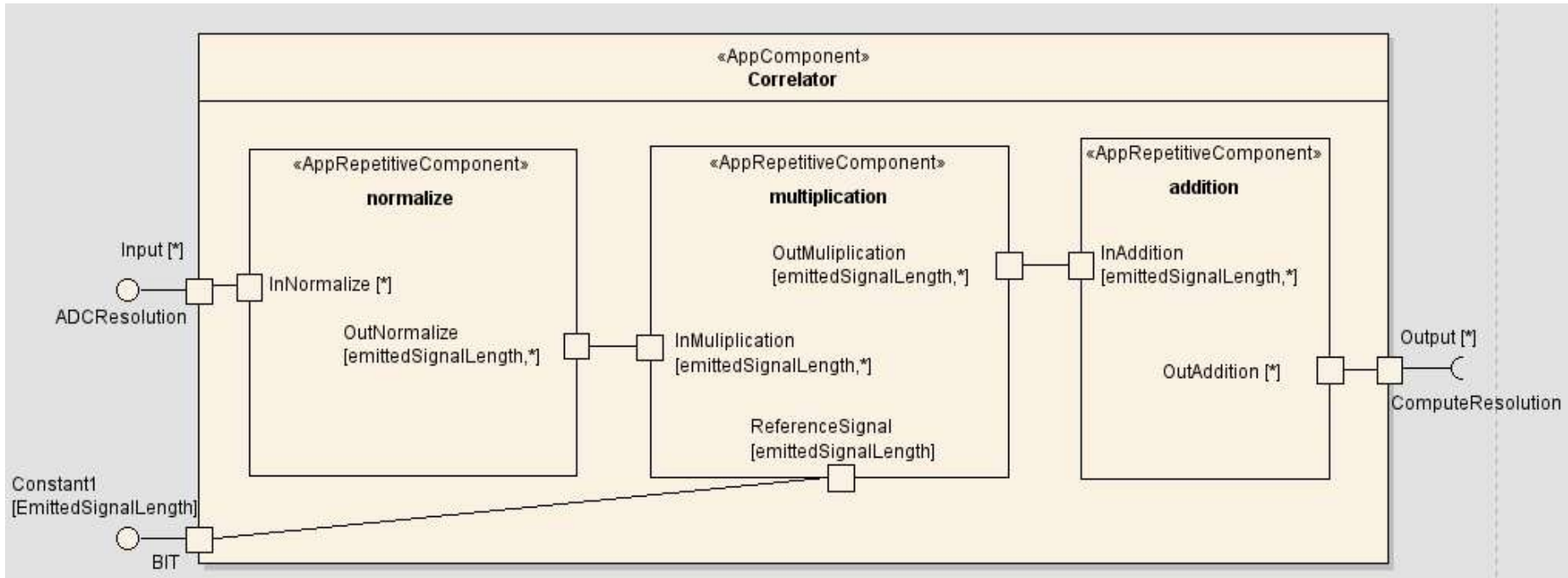


Radar signal

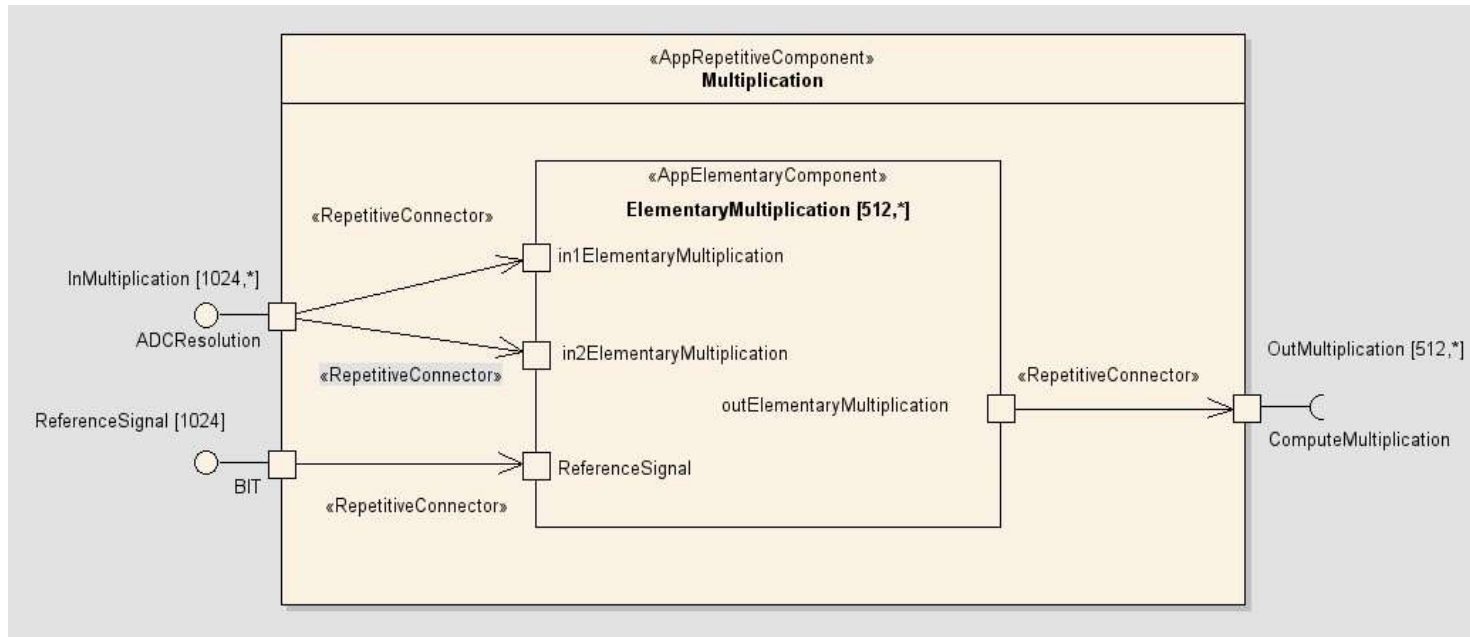


- Regular
 - NADD
 - ADD
- Except
 - Radar signal

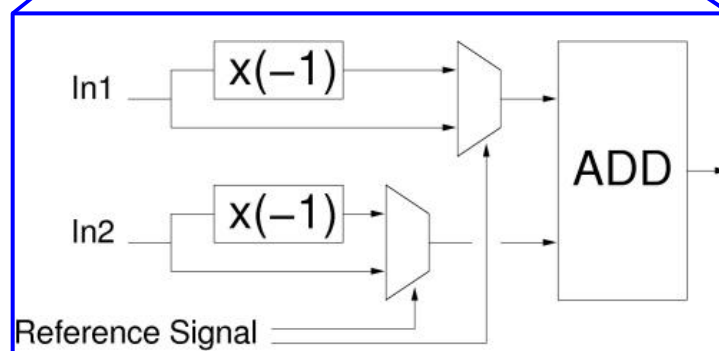
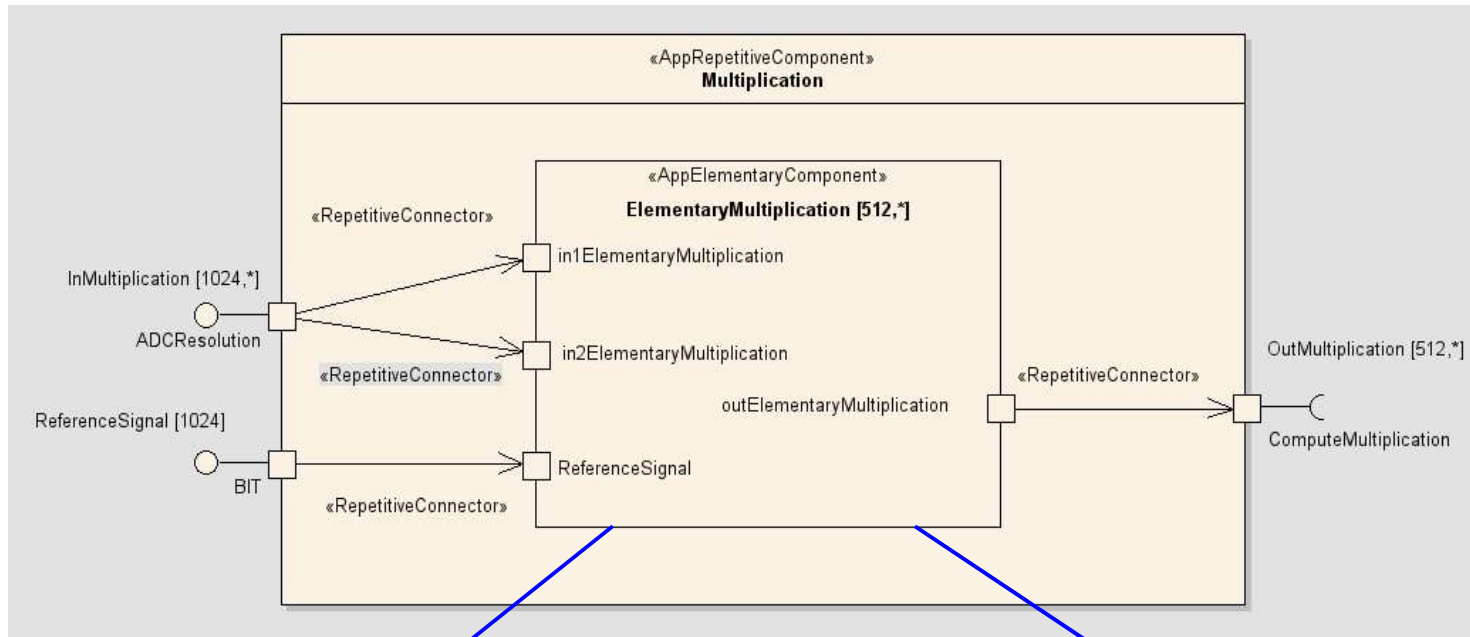
Correlator: UML side (1/3)



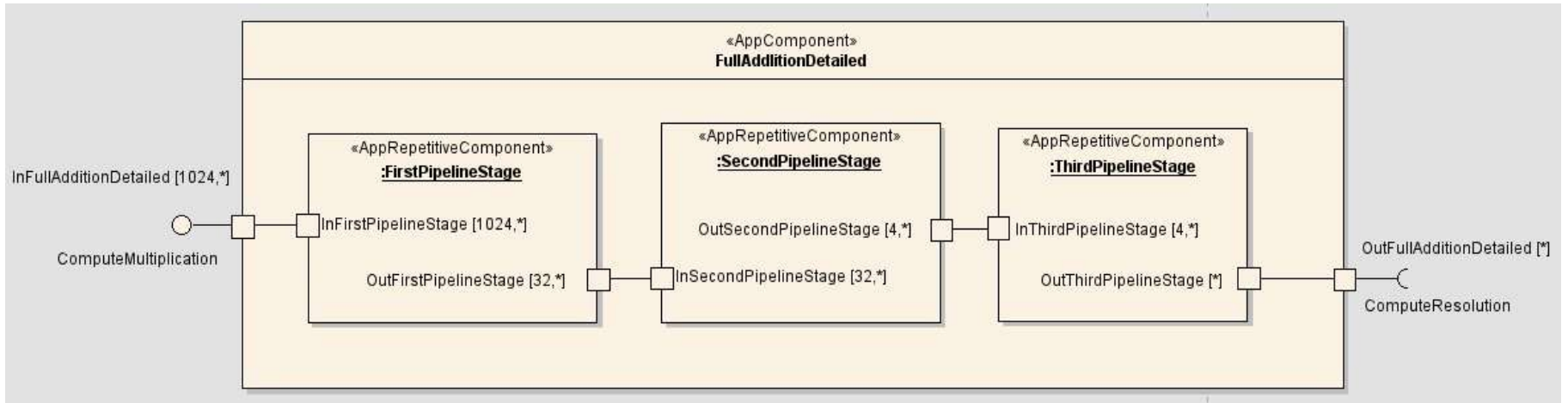
Correlator: UML side (2/3)



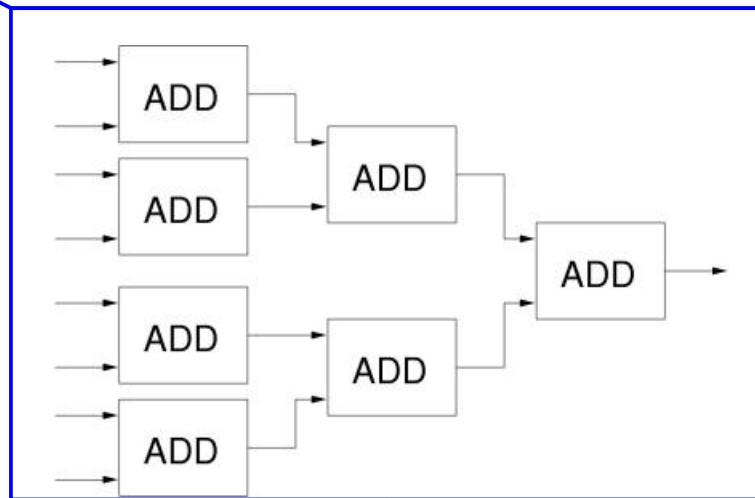
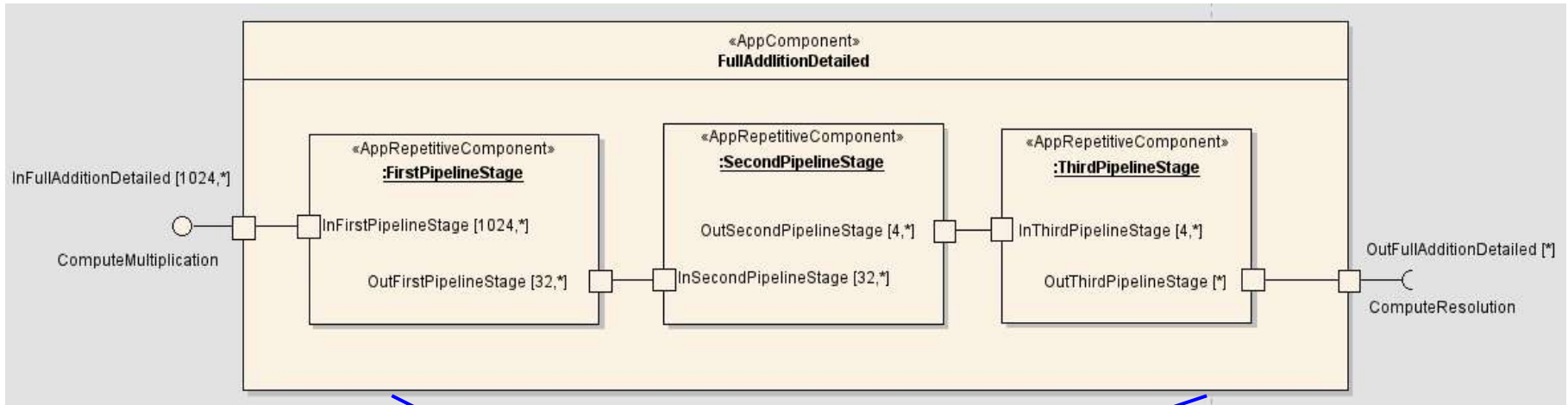
Correlator: UML side (2/3)



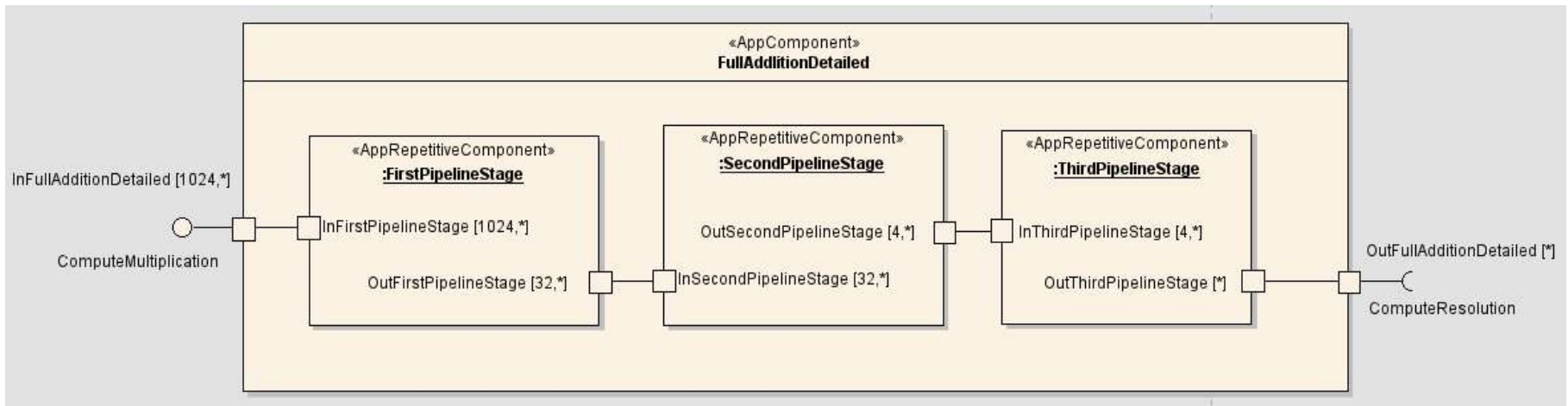
Correlator: UML side (3/3)



Correlator: UML side (3/3)



Correlator: UML side (3/3)



- But
 - Long to do
- Proposition
 - Elementary task with parameter for pipeline

Tugnait 3: algorithm side

- Objective
 - More powerful algorithm
- Formula

$$J_3(i_0) = \left| \sum_{j=0}^{N-1} C_{ccc}(j) \cdot C_{ccy}(j + i_0) \right|$$

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Constant

$$C_{ccy}(j) = \frac{1}{N} \sum_{i=0}^{N-1} c(i) c(i+1) y(i+j)$$

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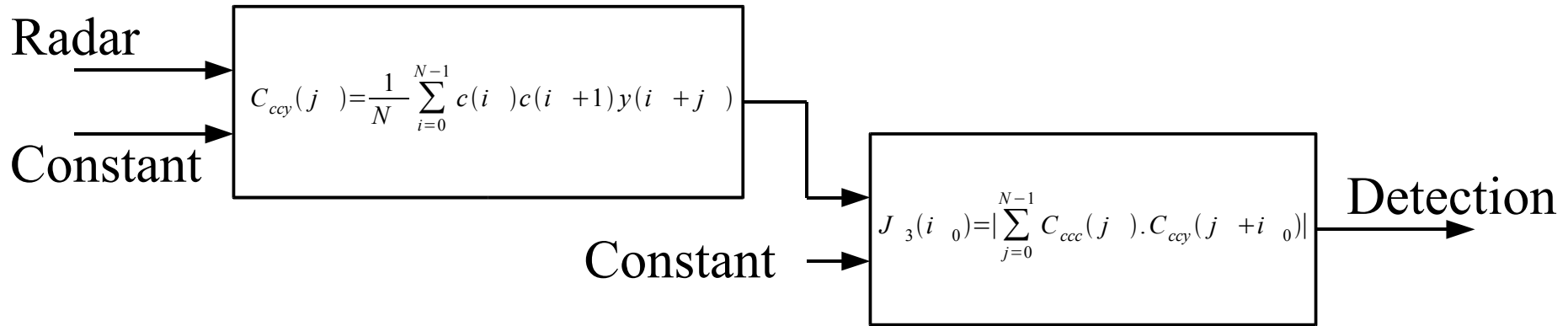
Constant

$$C_{ccy}(j) = \frac{1}{N} \sum_{i=0}^{N-1} c(i)c(i+1)y(i+j)$$

Constant

Radar

Tugnait 3: block side



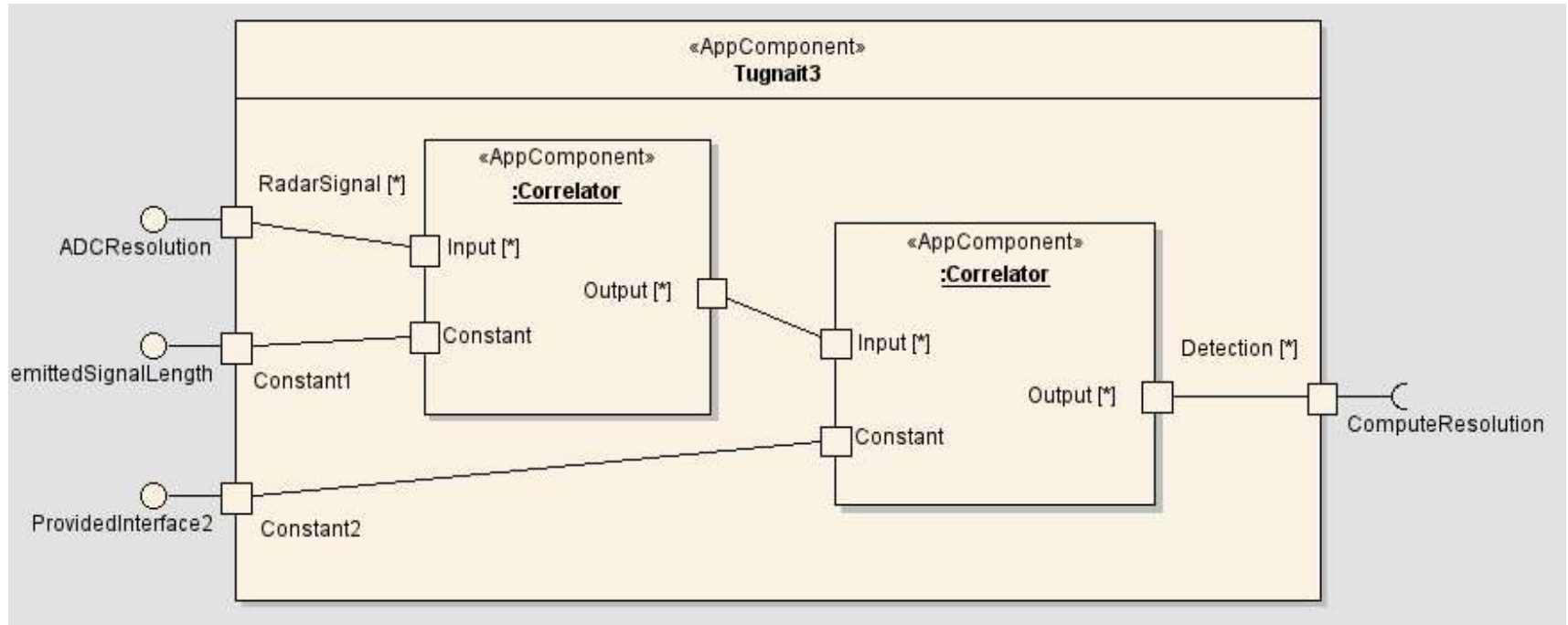
- Conclusion

- 2 instances of correlator algorithm to produce Tugnait 3 algorithm

- UML

- Easy to express...

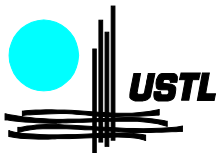
Tugnait 3: UML side



Characterization: global



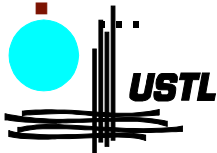
- Objective
 - Permit estimation of computation power required
- Way
 - Count each instance of each ET (Elementary Task)
 - Characterize each ET(number of operation)
 - Express computation power required by each ET



Characterization: example



- Multiplication step of correlator algorithm
 - Temporal constraints
 - Composed of 512*infinite instance NADD component
 - NADD (depend on resolution request)
 - Is composed of:
 - 2 multiplications,
 - 2 multiplexors,
 - 1 addition.
 - Require:
 - 27 Altera LE,
 - 28 Xilinx LC,

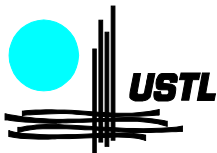


- Architecture part

Architecture part



- Isolate relevant and common characteristics of FPGA
 - Computation power: LE/LC, DSP blocks...
 - Data storage capability
 - Number Input/Output dedicated to user
 - Maximum frequency supported

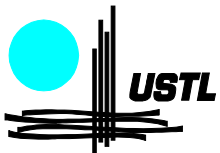


- Conclusion and perspectives

Conclusion



- Application
 - Modeling possible in ArrayOL
- Architecture
 - Enrich current architecture meta-model with FPGA is feasible



Perspective



- Application
 - Validate model (13 july?)
 - Characterize it (implementation test)
- Architecture
 - Chose representative FPGA in order to create data base

