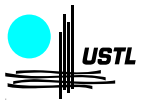
Transformation towards FPGA

Sébastien Le Beux
Laboratoire d'informatique fondamentale de Lille
Université des sciences et technologies de Lille



8 November 2006

Introduction

Several key words

- Data parallel application
- FPGA
- Transformation

Context

Gaspard2 MM

Hardware Accelerator MM

Publications

Gaspard

- Application, architecture, association, deployment...
- faire la ligne Magicdraw/UML et Eclipse

Gaspard in ModEasy

- In UML:
  - Application: a detection algorithm
  - Architecture: a hardware accelerator
  - Association: the whole algorithm onto a hardware accelerator
  - Deployment: the hardware accelerator on a FPGA and the application elementary tasks in VHDL
- Transformation
  - Consumes the interesting subset
  - Produces a hardware accelerator
- In Eclipse
  - A hardware accelerator model
  - VHDL code generation

Context

Gaspard2 MM

Hardware Accelerator MM

Publications

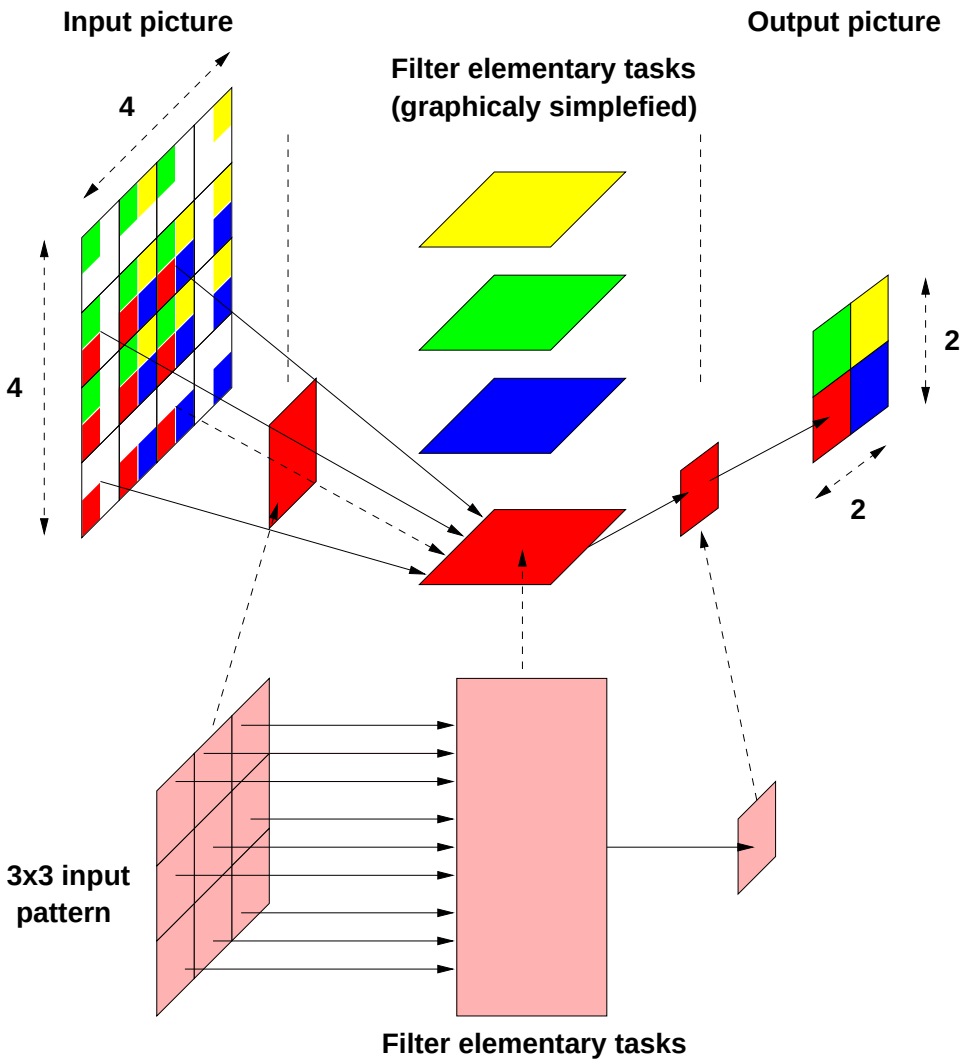
Repetition in Gaspard2 MM

- Repetitive component is a structural component and contains
  - Inputs and outputs ports
  - A repeated component instance
  - Tilers
- Tiler (based on Array-OL) is a particular connector and is composed of
  - Source port or portInstance
  - Target port or portInstance
  - Tiling description (origin, paving, fitting)

Gaspard2 MM

Demonstration...

A model



A model in UML

Repetition in Hardware Accelerator MM

- Repetitive component is a structural component and contains
  - Inputs and outputs ports
  - A repeated component instance
  - Tilers (hardware tiler!!)
- Tiler is an elementary component
  - Generated from tiling description
  - Contains one input and one output port
  - Is connected to its environment within connector

The Hardware Accelerator MM

Demonstration...

A model

A produced VHDL code (1/2)

```
ENTITY average IS
    PORT(
        clk: IN STD_LOGIC;
        raz : IN STD_LOGIC;
        inpixel_temp: IN consumned_pixelin;    --(4,4)
        outpixel: OUT produced_pixel);         --(2,2)
END average;

ARCHITECTURE structural OF average IS

signal my_inputs_pattern : produced_input_pattern; --(2,2,3,3)
signal my_outpixel: produced_output_pixel;         --(2,2)

BEGIN
        ---------------------------------------------------------------------
        -- input tiler instantiation and mapping
        ---------------------------------------------------------------------
        instTilerIn: TilerIn
                port map(
                    clk => clk,
                    raz => raz,
                    inTiler=> inpixel_temp,          --(4,4)
                    outTiler=>my_inputs_pattern);    --(2,2,3,3)
```

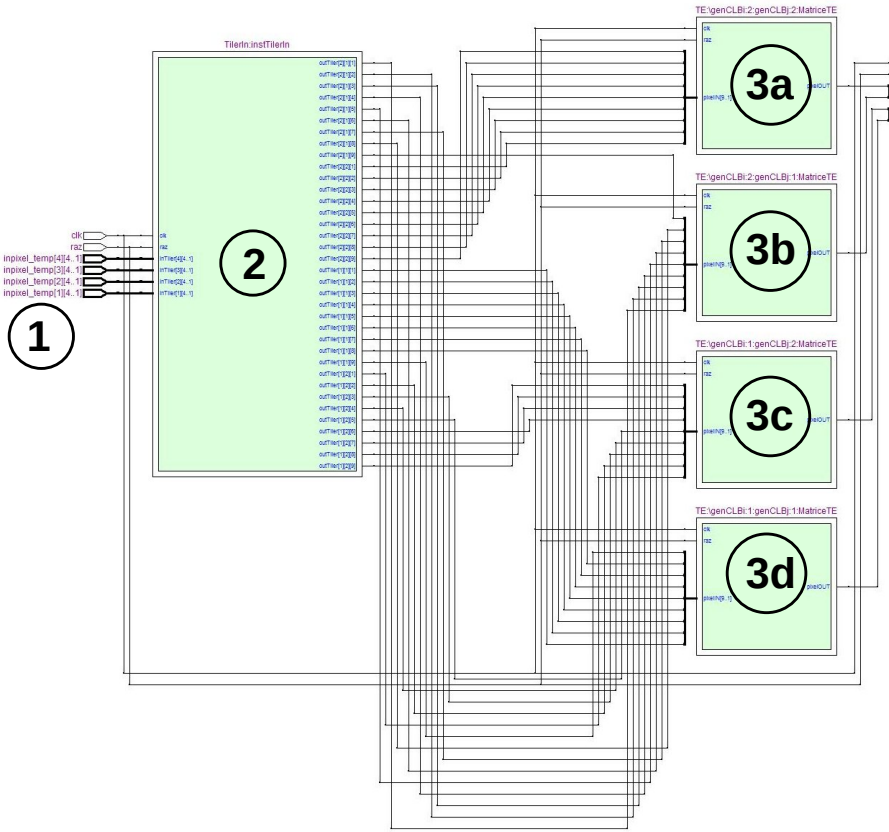
A produced VHDL code (2/2)


```
        ------------------------------------------------------------------------
        -- loops for elementary tasks iteration
        ------------------------------------------------------------------------
        genCLBi : for i in 1 to 2 generate
            genCLBj : for j in 1 to 2 generate
                MatriceTE: TE
                    port map (
                        clk => clk,
                        raz => raz,
                        pixelIN => my_inputs_pattern(i)(j), --(2,2,3,3)
                        pixelOUT => my_outpixel(i)(j));     --(2,2)
            end generate;
        end generate;

        ------------------------------------------------------------------------
        -- output tiler instantiation and mapping
        ------------------------------------------------------------------------

        instTilerOut: TilerOut
                port map(
                    clk => clk,
                    raz => raz,
                    inTiler=> my_outpixel, --(2,2)
                    outTiler=>outpixel);   --(2,2)
END structural;
```

A synthesis result



1. **Ports of repetitive**
2. **Input Tiler**
3. **Elementary Task instance**
4. **Ouput Tiler**
5. **Ports of repetitive**

Context

Gaspard2 MM

Hardware Accelerator MM

Publications

Publication(s?) in ModEasy

- Some publication in each teams...
- But no common publication
  - Workshop MARTES: refused because "*not a real contribution, just a merge of 2 previous contribution*". Shall we try again?
  - EURASIP: submission in progress... but the only one...
- Problems encountered:
  - Word vs Latex !!!!
  - Find a real common contribution
  - Not motivated?