Modélisation compositionnelle d'architectures GALS dans un modèle de calcul polychrone

(Compositional modeling of GALS architecture in a polychronous model of computation)

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Embedded systems

Application domains

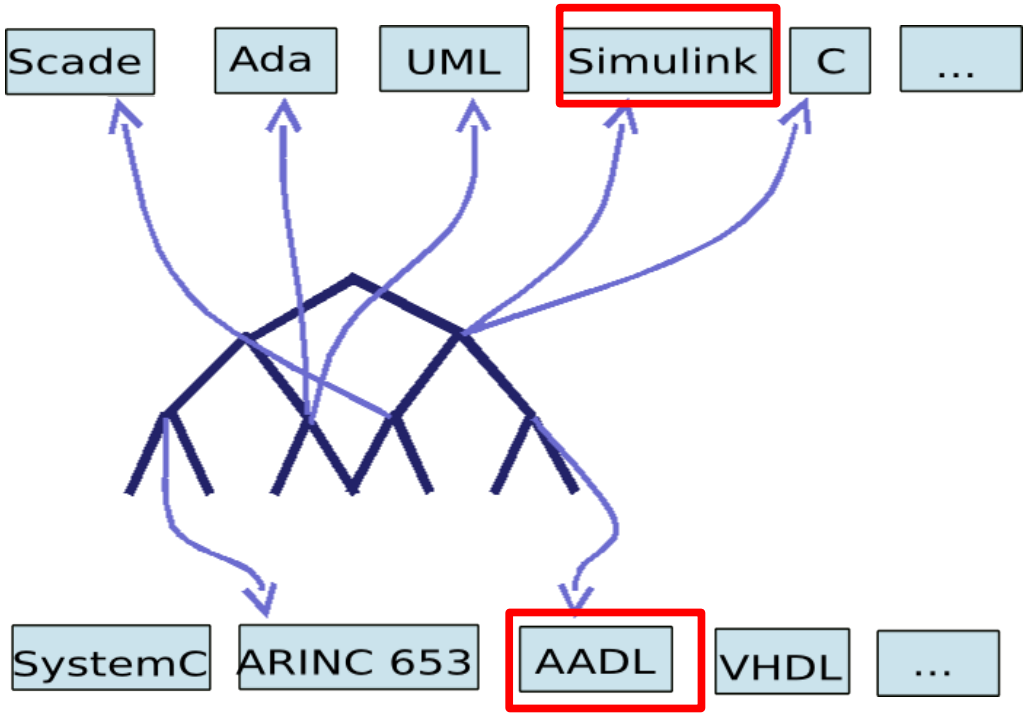
- Avionics, automobile, telecommunications, ...

Embedded systems design

- Design methodology
  - Modular design
  - System level co-design
  - GALS
- Modeling & design language
  - UML, AADL, SystemC, ...
- Problems: determinism, property verification, ...

Motivation (1)

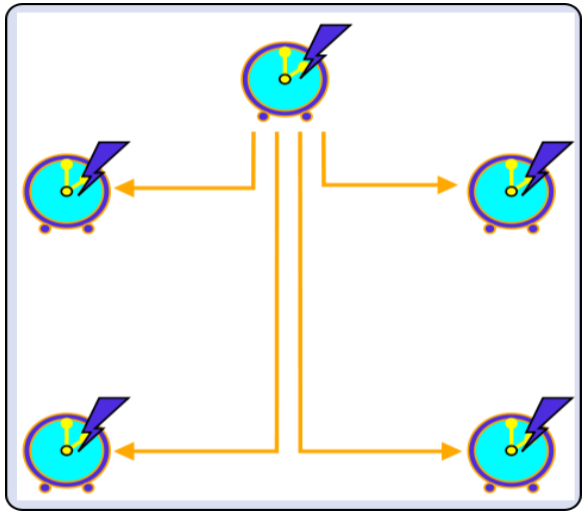
- Co-modeling
- Validation



Motivation (2)

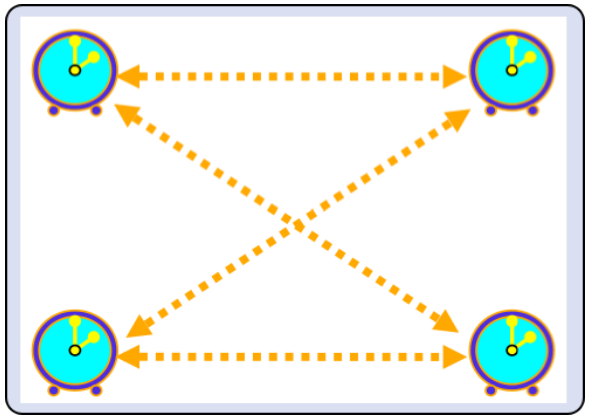
Synchronous models of computation

- Master clock
- Lustre, Simulink, ...



Asynchronous models of computation

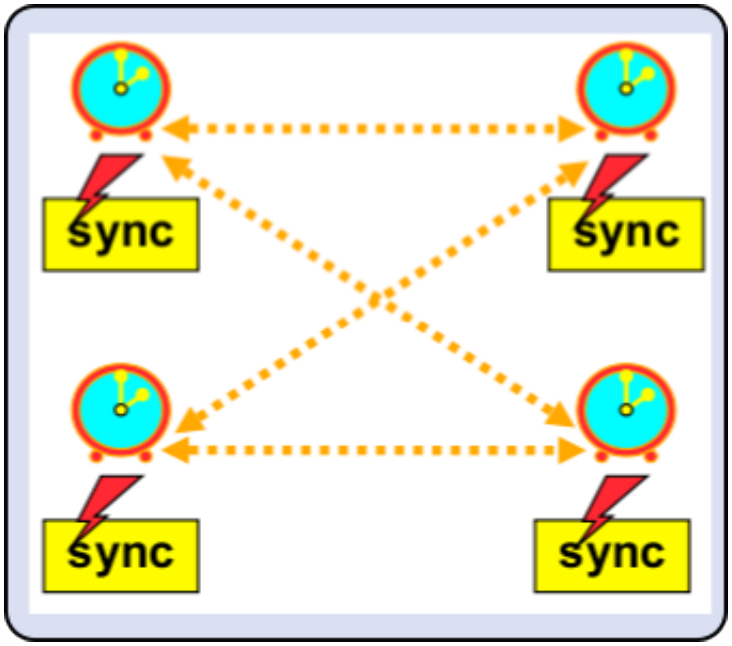
- No global clock
- UML, SysML, ...



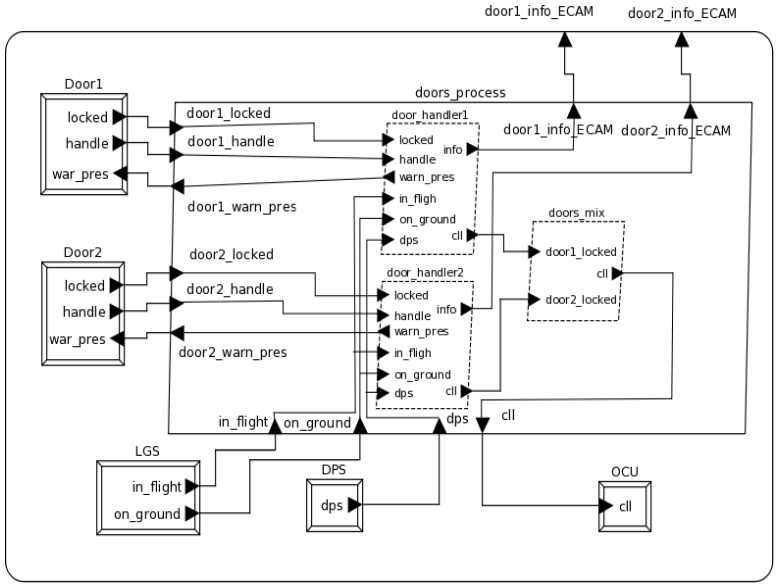
Motivation (3)

Polychronous model of computation

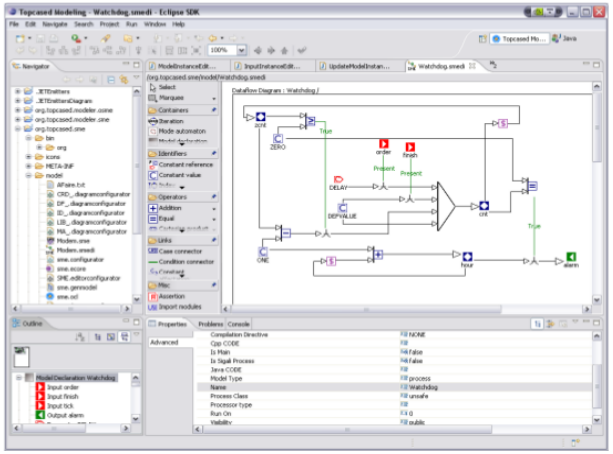
- Composing modules
- Each module is a synchronous software
- No master clock
- Clocks are related to synchronization constraints



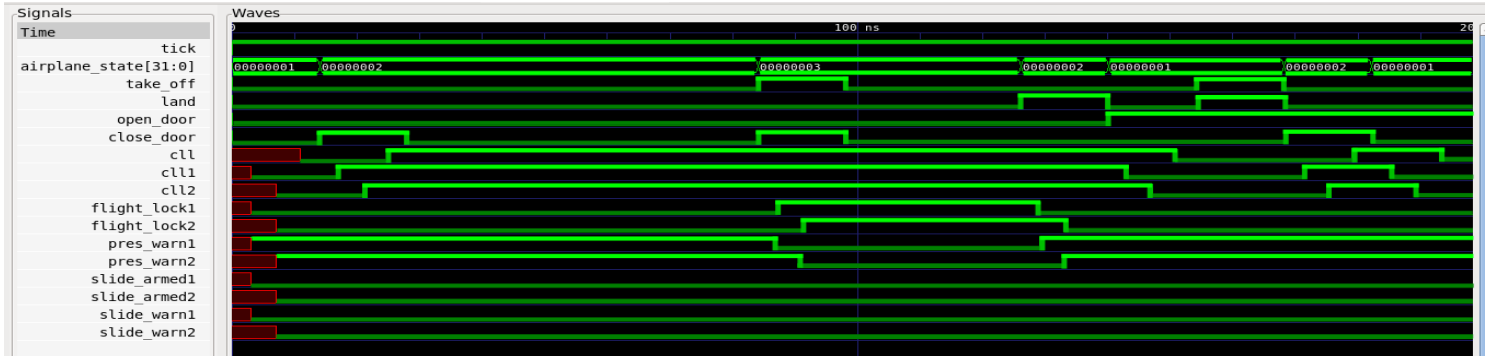
Proposition of this work



Modeling



Simulation & validation

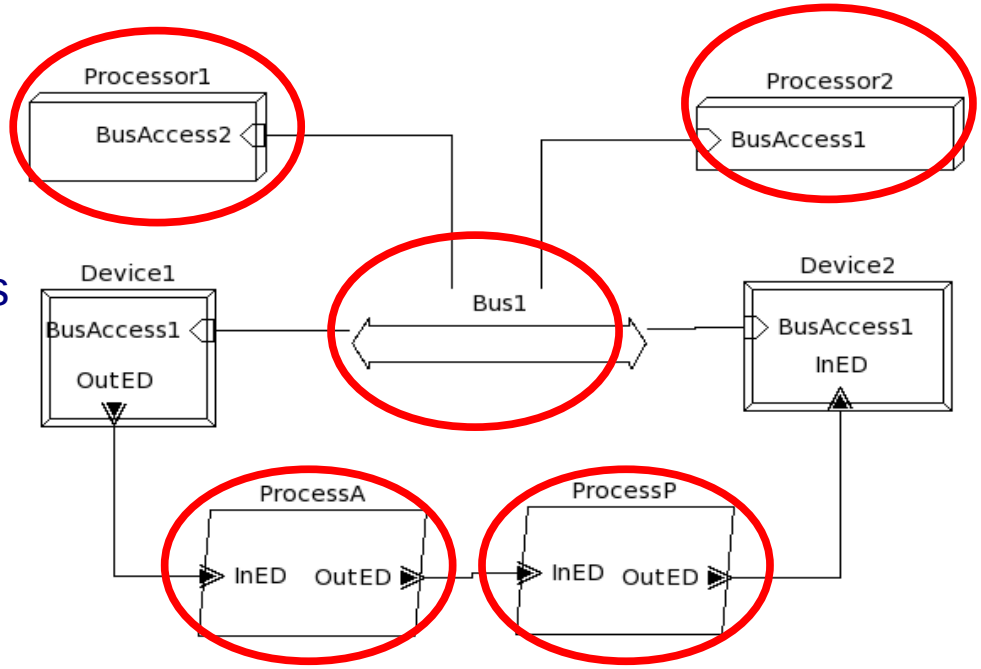


Outline

- Context
  - AADL specification
  - Signal language and Polychrony
- Contributions
- Case study
- Perspectives and conclusions

Architecture Analysis and Design Language

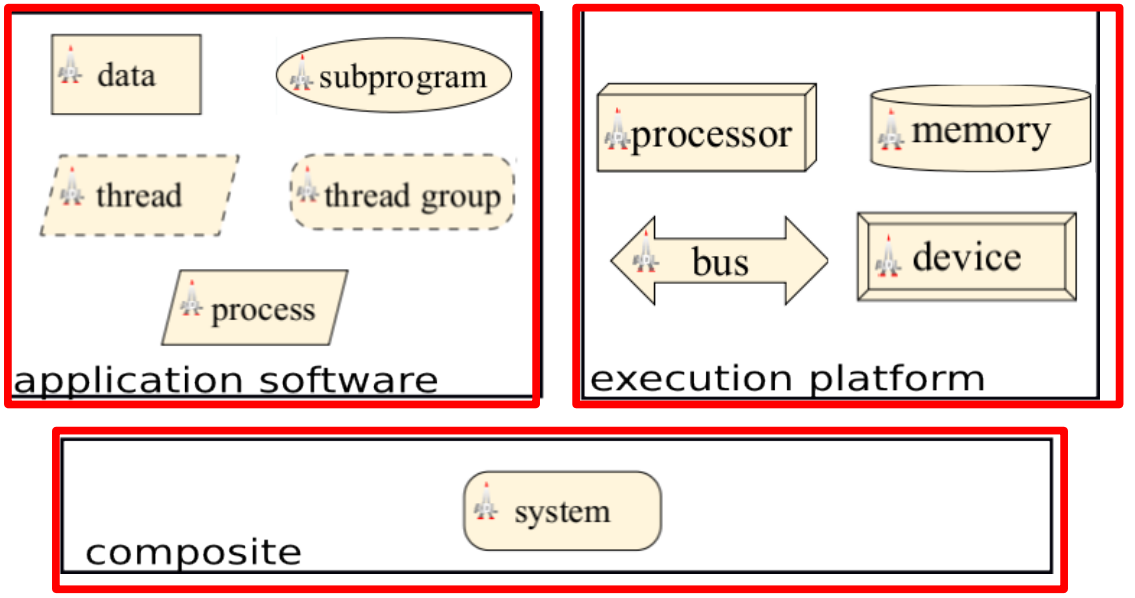
- SAE standard
- Design and evaluation of architecture of embedded systems
- Assembly of software mapped to execution components



AADL

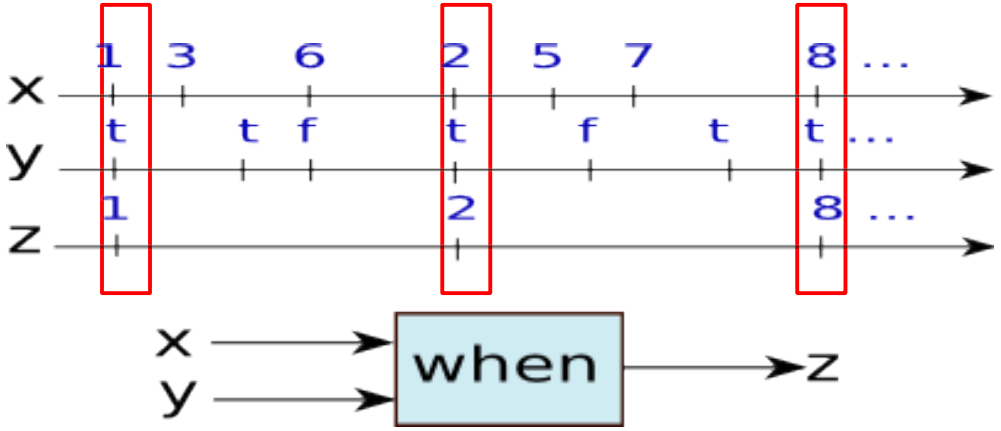
Component-based architecture

- Application software
- Execution platform
- Composite



Signal – a multi-clocked data-flow language

- Formal specification of embedded real-time systems
- Model of computation suitable for GALS
- Polychronous model of computation: multi-clocked



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  - Modeling AADL components in Signal
  - Distributed model generation
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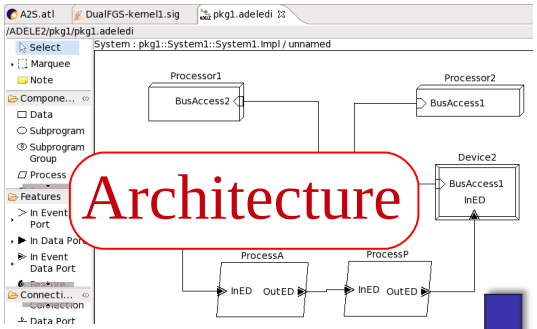
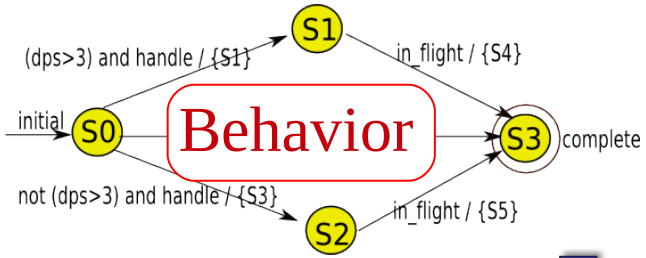
Proposed approach

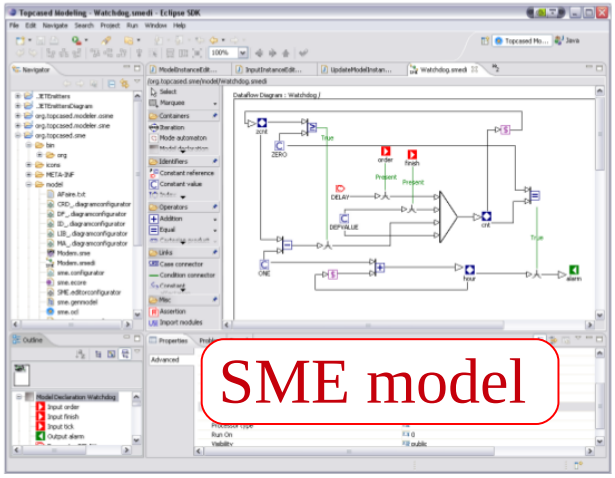
Modeling AADL in Signal

- Architecture components
- Behavior specifications
  (Behavior Annex, Simulink ...)

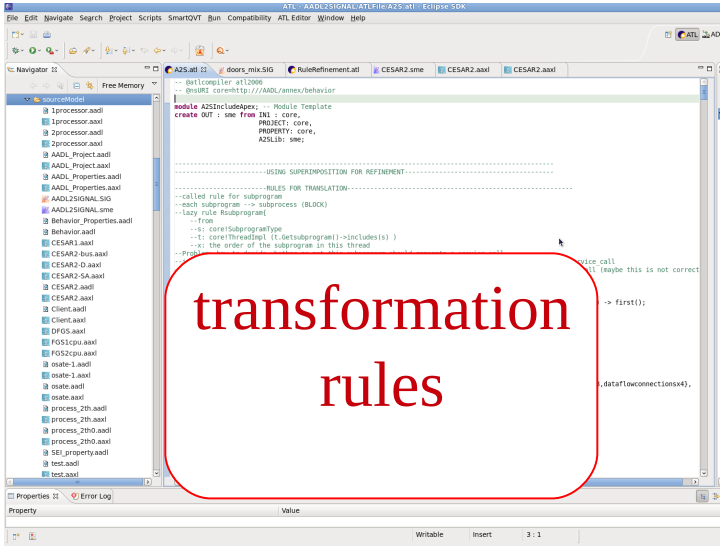




Polychrony



TopCased



From abstract logical time to more concrete simulation time (1)

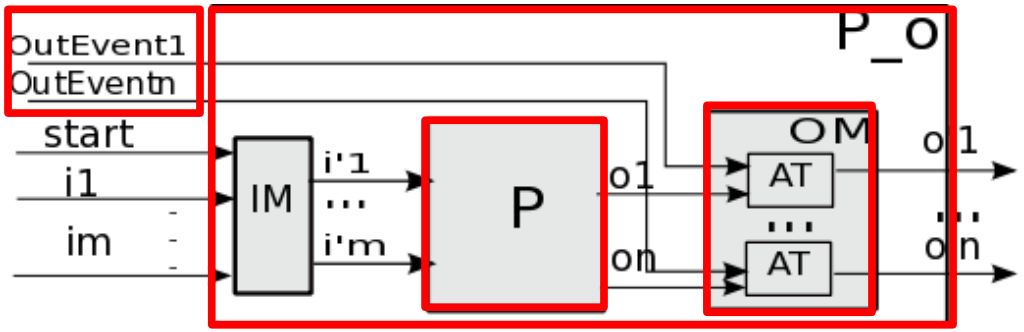
Modeling computation latencies

- Synchronous program: logical instantaneous execution
- AADL model: computation for a specified time interval
- Adapter: interface different timing semantics

P: process

P_o: container

OM: (output) “memory” process

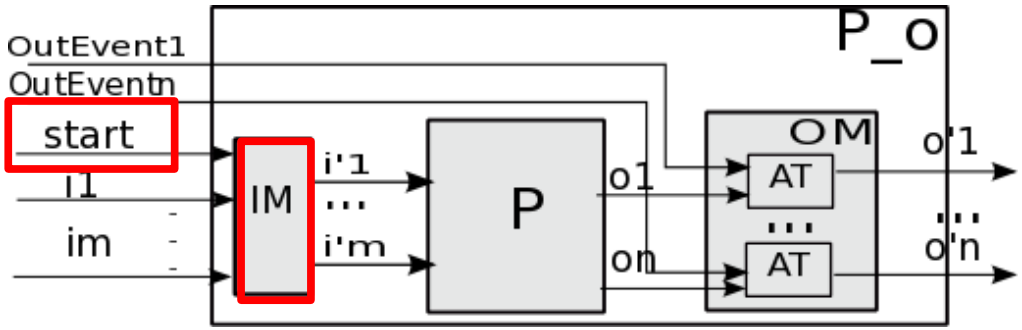


From abstract logical time to more concrete simulation time (2)

Modeling propagation delays

- Synchronous program: instantaneous communication
- AADL model: received input could be memorized
- Activation signal

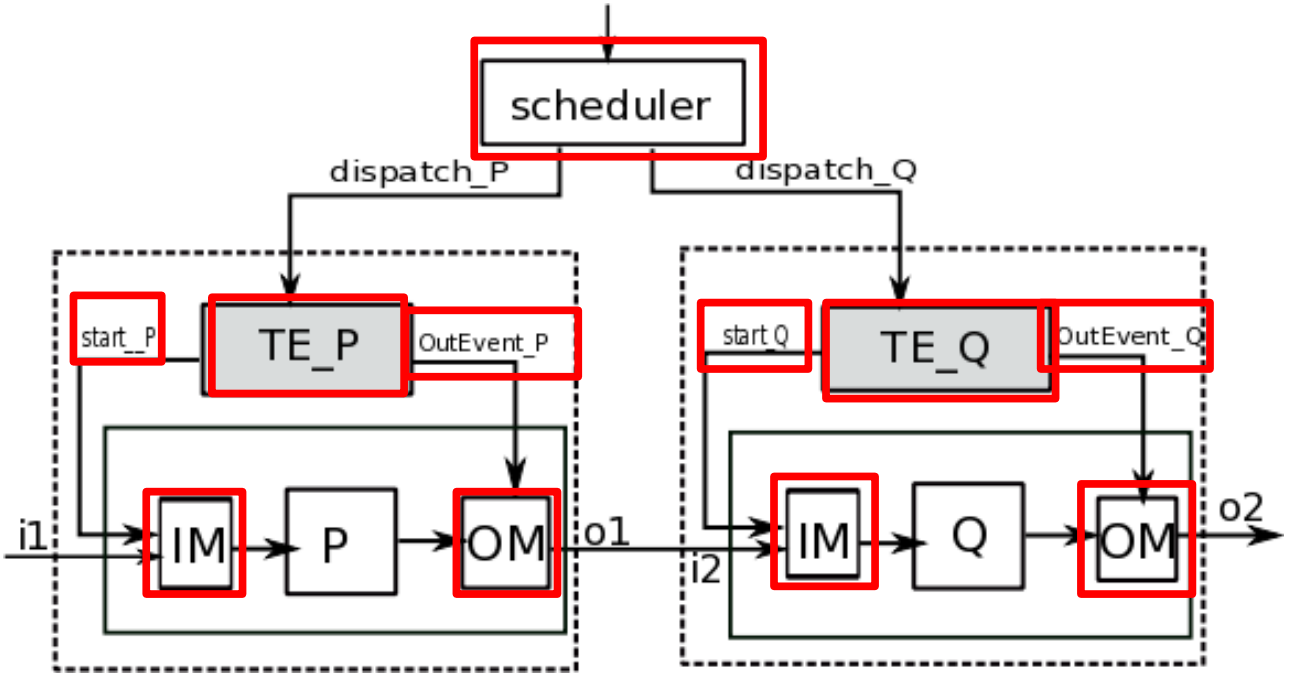
IM: (input) “memory” process



From abstract logical time to more concrete simulation time (3)

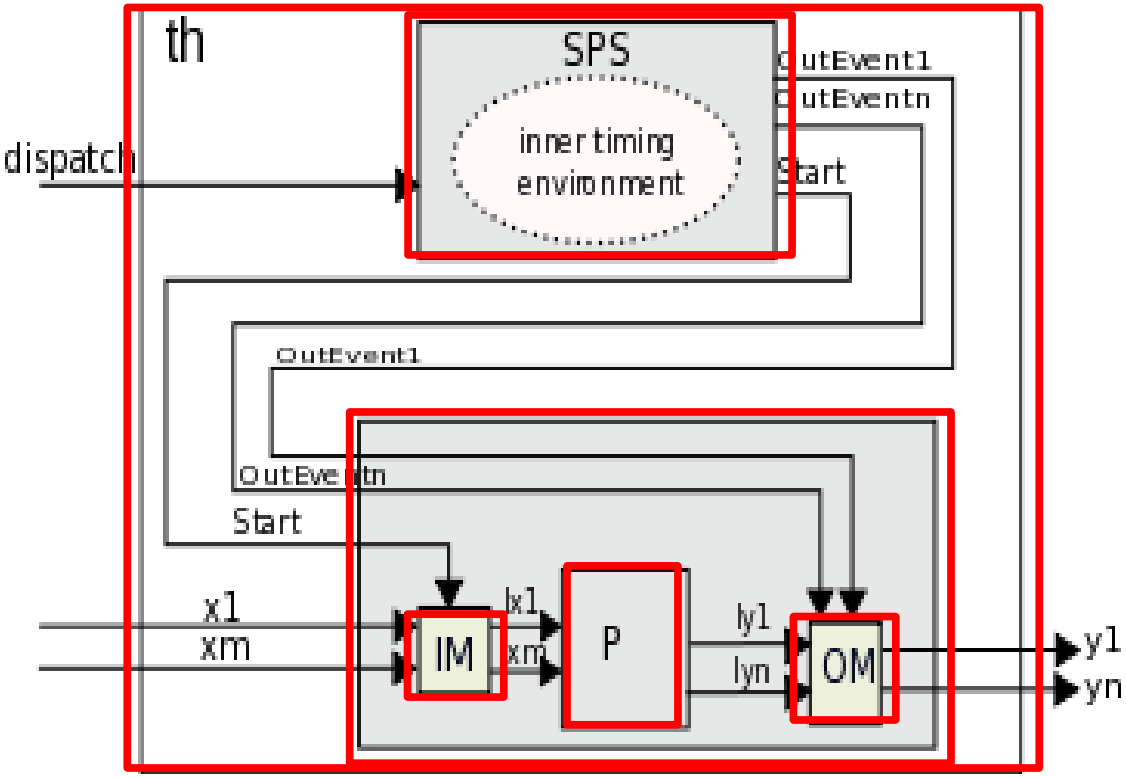
Towards modeling time-based scheduling

- How to control the activation and delay conditions
- How to generate these conditions
- Timing environment



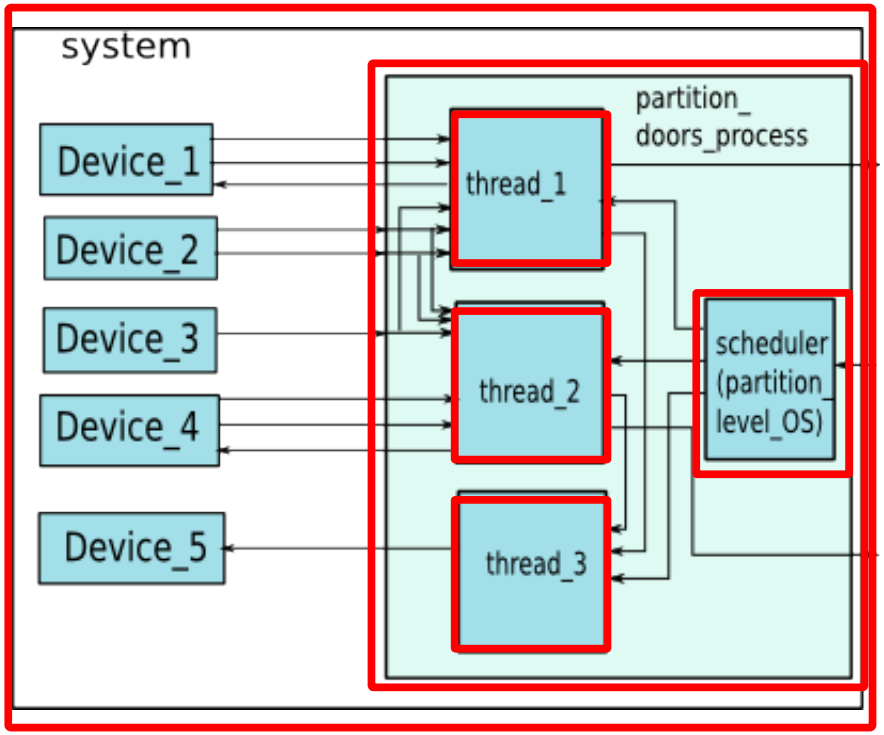
Thread modeling

- Synchronous interpretation
- Synchronization and activation container
- “Memory” process
- Timing environment



Components implemented in this work

- Software
  - Thread
  - Process
  - Subprogram
  - Data
- Hardware
  - Processor
  - Bus
  - Device
- System



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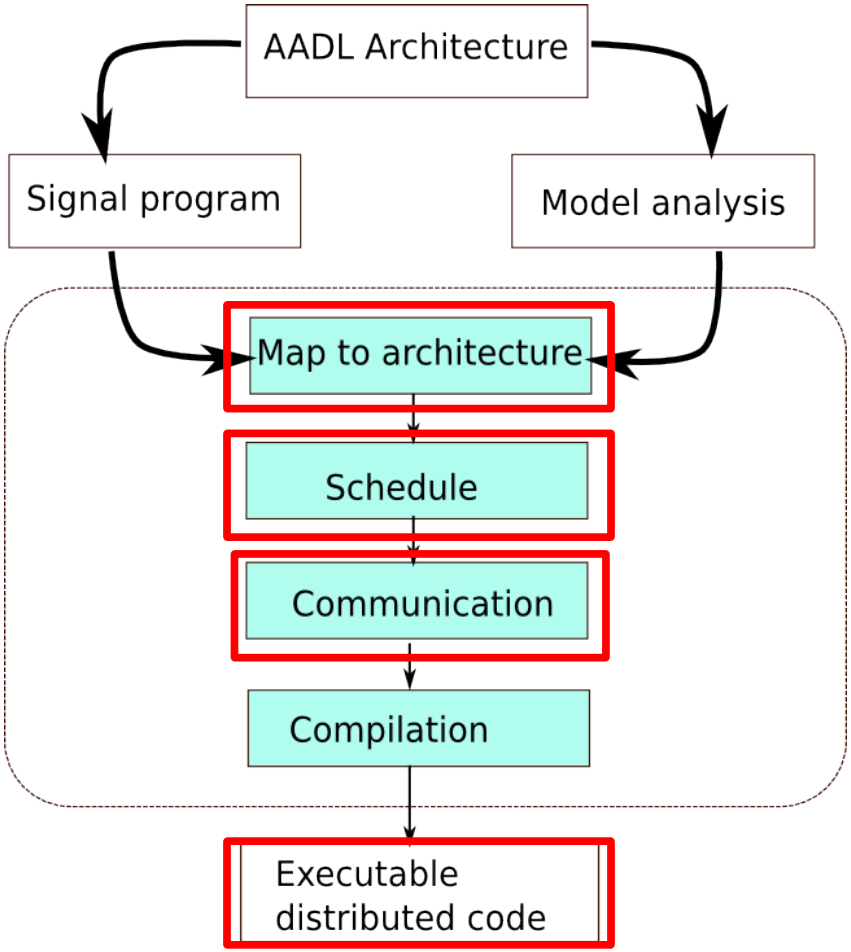
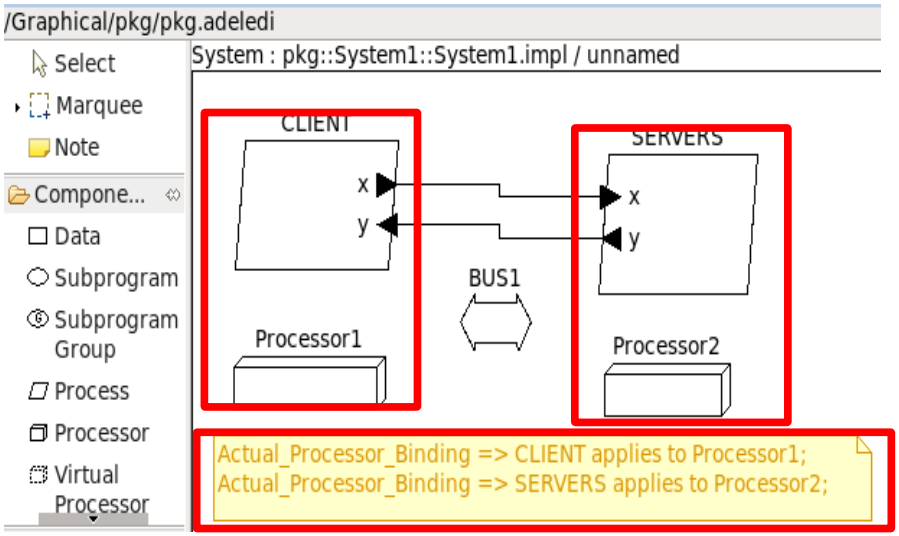
Virtual prototyping of distributed code generation

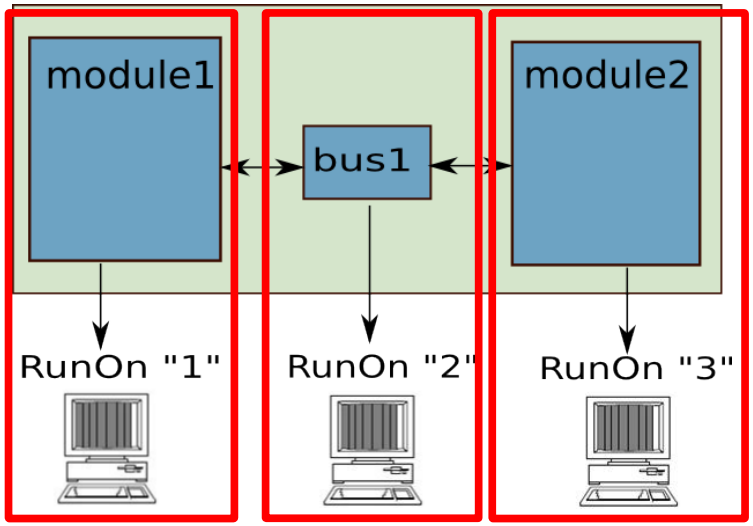
- Distribute to execution platform
- Schedule of processes in each separated part
- Add communication



A distribution example

- Distribution properties
- Assign each module to a different processor
- Scheduling
- Communication





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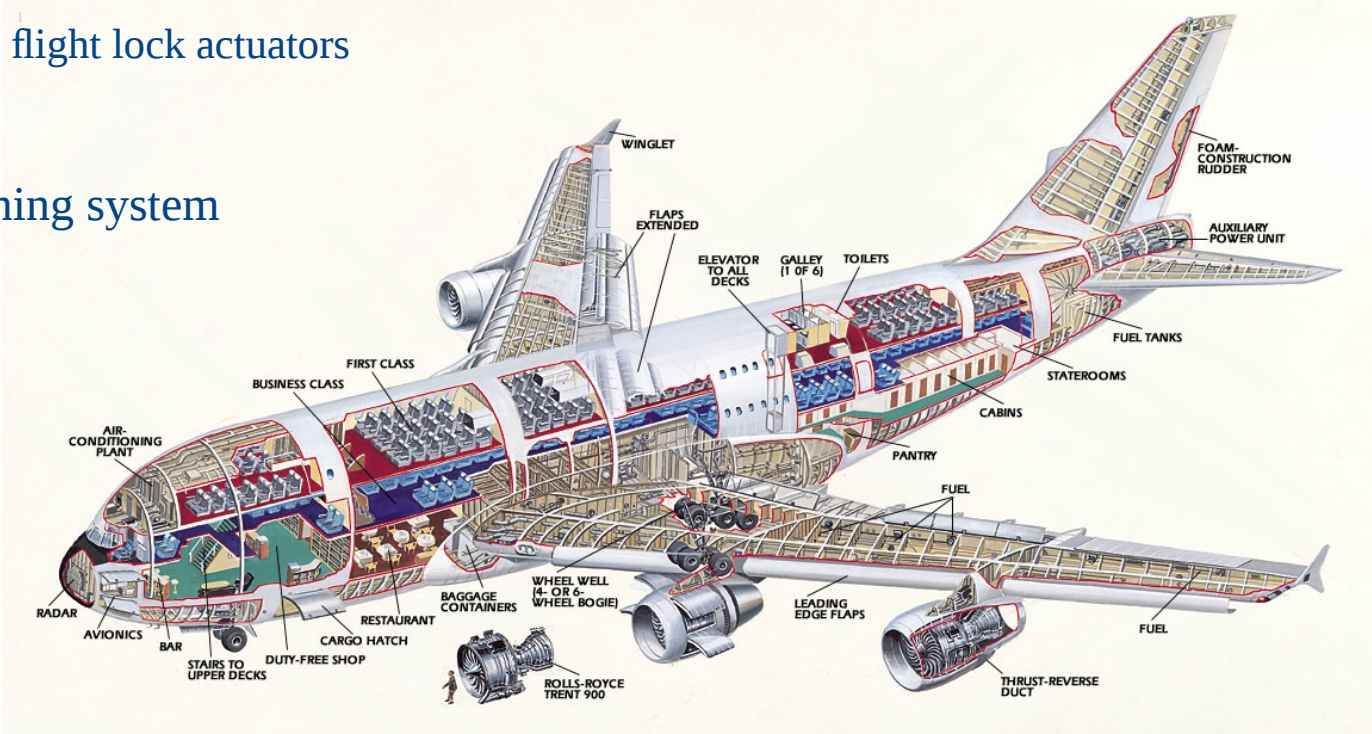
A350 Doors Management System

Flight control systems

- Landing gear system
- **Doors management system**
  - passenger doors, emergency exits, cargo doors
  - Monitor doors status via door sensors

    Control flight lock actuators

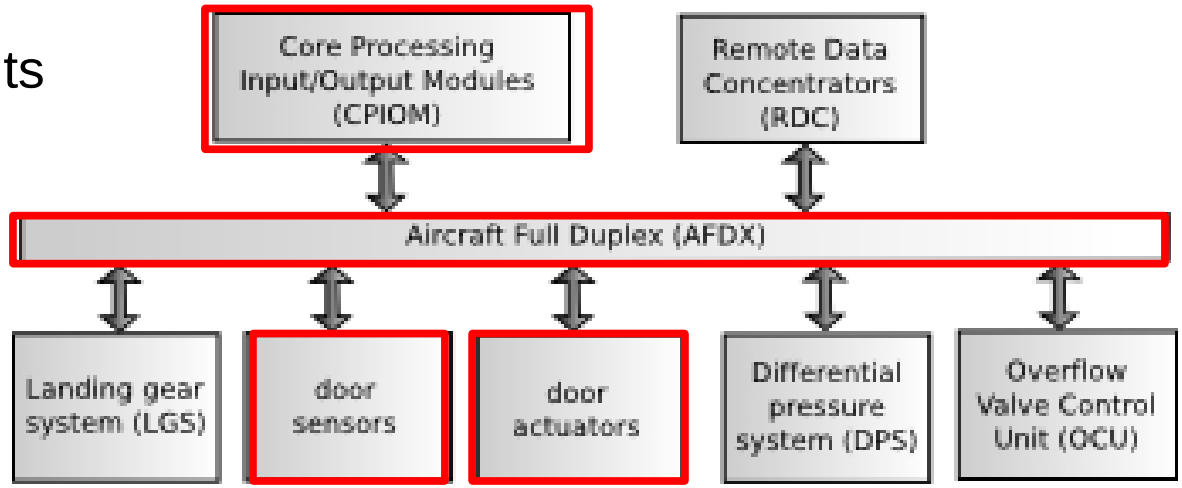
    ...
- Flight warning system
- ...



Simplified Doors and Slides Control System

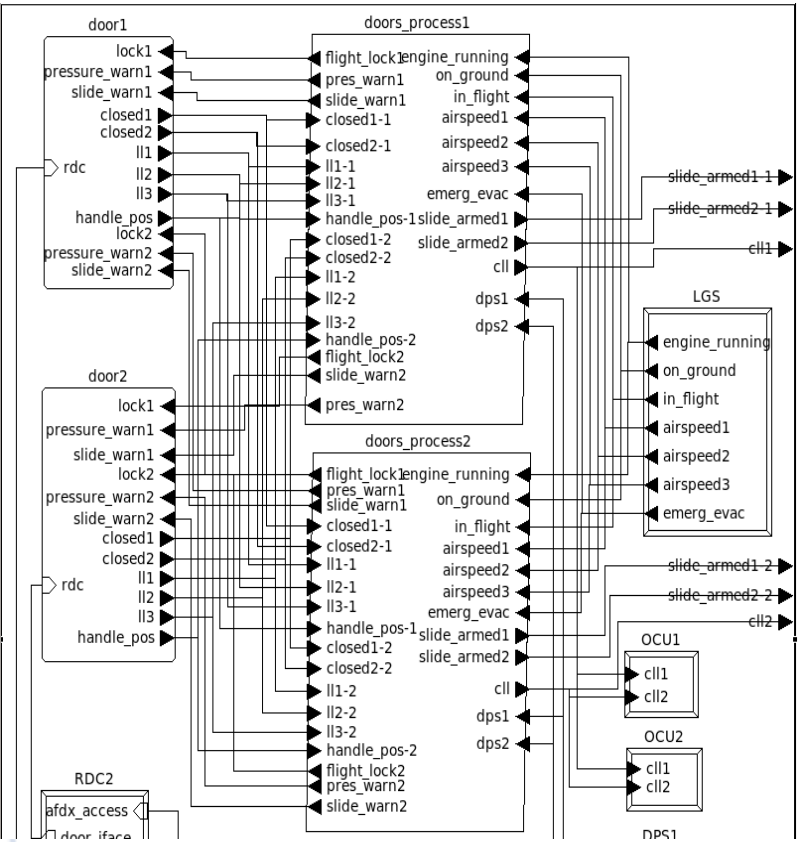
- Software component
  - monitor door status
  - control flight lock

- Hardware equipments
  - Door actuators
  - Door sensors
  - AFDX bus



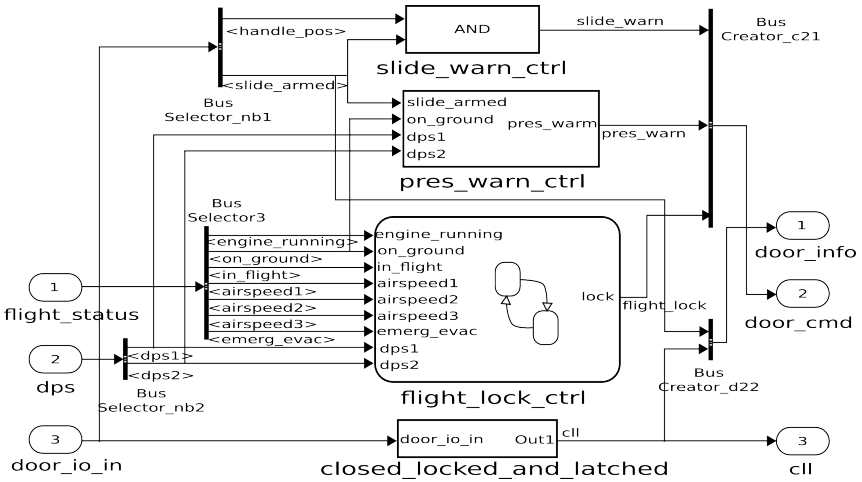
Co-modeling

AADL



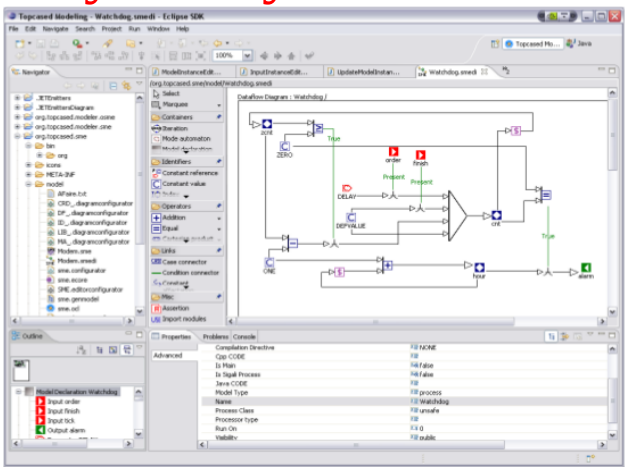
Asynchronous structural specification

Simulink



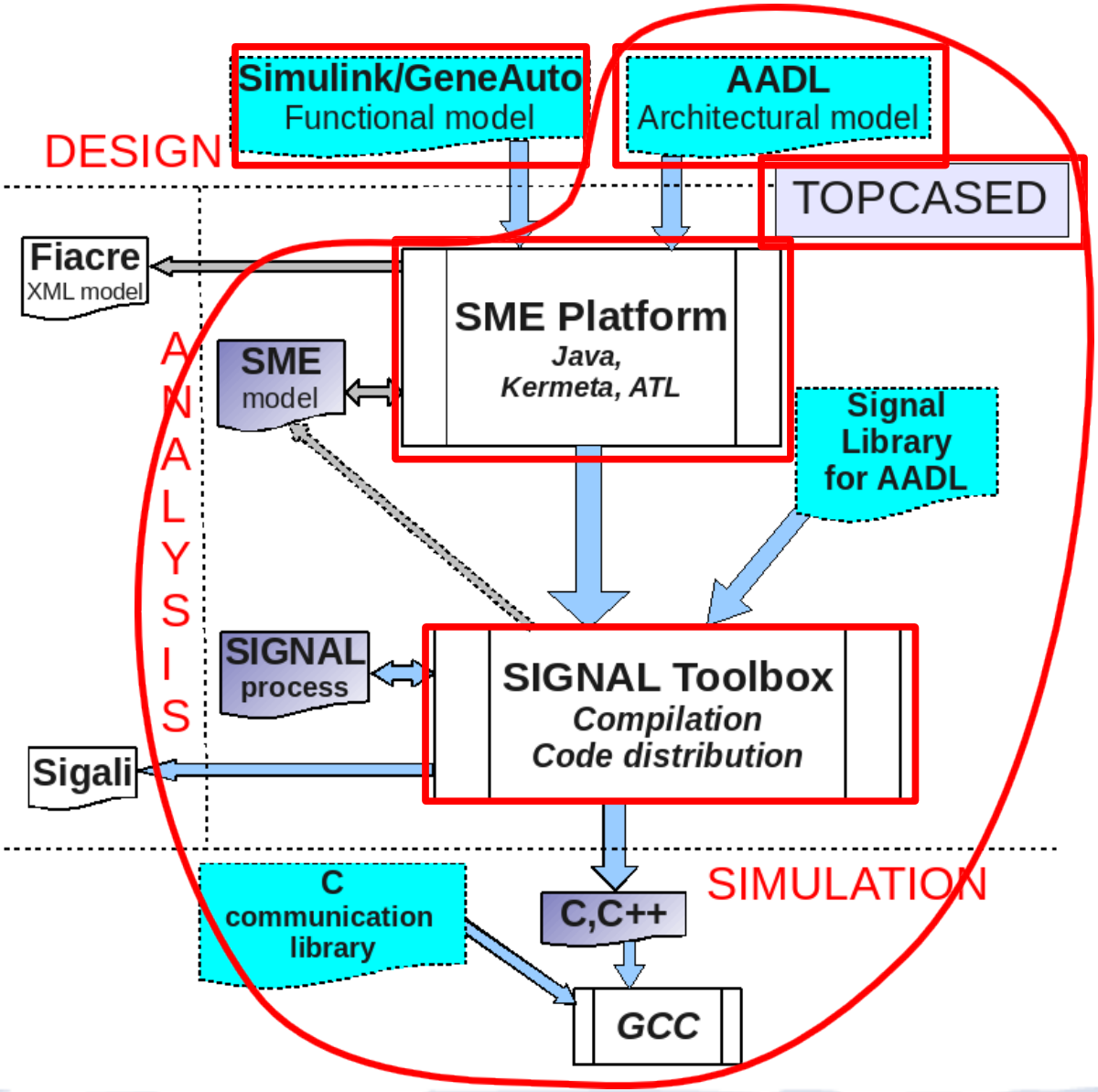
Synchronous functional specification

Polychrony



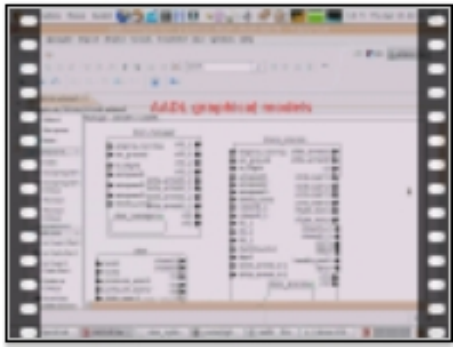
GALS simulation model

Global view of co-design



Simulation

- System modeling
- Formal transformation
- System composition
- VCD-based simulation



Conclusions and perspectives

Conclusions

Polychronous modeling of a subset of AADL model

- Formal interpretation of AADL components
- An effective method for modeling and validation of GALS architecture

Distributed code generation

- Distribute code to different processors

Formal verification, simulation and analysis

- A case study for co-modeling and simu

Perspectives

Extension of the modeling

- Cover a larger subset of AADL
- Dynamic scheduling model and schedulability analysis

Extension of validation

- Test case generation